

# EG915U-EU

# Hardware Design

**LTE Standard Module Series**

Version: 1.0.0

Date: 2021-09-08

Status: Preliminary



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## Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.



Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.



Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.



Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.



Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.



The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.



In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

# About the Document

## Revision History

Version	Date	Author	Description
-	2021-09-08	Ailsa WANG/Reuben WANG	Creation of the document
1.0.0	2021-09-08	Ailsa WANG/Reuben WANG	Preliminary

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# 1 Introduction

This document defines the EG915U-EU module and describes its air interfaces and hardware interfaces which relate to customers' applications.

It can help customers quickly understand interface specifications, electrical and mechanical details, as well as other related information of the module. Associated with application notes and user guides, customers can use this module to design and to set up mobile applications easily.

## 1.1. Special Mark

**Table 1: Special Mark**

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of such model is currently unavailable.

## 2 Product Overview

The module is an LTE-FDD/GSM module, supports LTE-FDD, GSM/GPRS network data connection. It also provides voice functionality, Bluetooth and Wi-Fi Scan for customer's specific applications. Related information and details are listed in the table below:

**Table 2: Brief Introduction of the Module**

Categories	
Packaging and pins number	LGA; 126
Dimensions	(23.6 ±0.2) mm × (19.9 ±0.2) mm × (2.4 ±0.2) mm
Weight	2.5 ±0.2 g
Wireless network functions	LTE/GSM/Bluetooth/Wi-Fi Scan

### NOTE

1. EG915U-EU supports Bluetooth and Wi-Fi Scan functions.
2. Because of common antenna interfaces, two functions cannot be used at the same time.

## 2.1. Frequency Bands and Functions

Table 3: Wireless Network Type

Wireless Network Type	EG915U-EU
LTE-FDD	B1/B3/B5/B7/B8/B20/B28
GSM	850/900/1800/1900 MHz
Bluetooth/Wi-Fi Scan <sup>1</sup>	2.4 GHz

## 2.2. Key Features

Table 4: Key Features

Parameter	Details
Power Supply	<ul style="list-style-type: none"> <li>Supply voltage: 3.3–4.3 V</li> <li>Typical supply voltage: 3.8 V</li> </ul>
SMS	<ul style="list-style-type: none"> <li>Text and PDU mode.</li> <li>Point-to-point MO and MT.</li> <li>SMS cell broadcast.</li> <li>SMS storage: Stored in the (U)SIM card and ME, ME by default.</li> </ul>
(U)SIM Interface	Supports (U)SIM card: 1.8 V, 3.0 V.
Audio Features	<ul style="list-style-type: none"> <li>Supports two analog audio interfaces: one analog audios input and one analog audios output.</li> <li>GSM: HR/FR/EFR/AMR/AMR-WB.</li> <li>Support echo cancellation and noise suppression</li> </ul>
PCM Interface	<ul style="list-style-type: none"> <li>One PCM interface.</li> <li>Used for audio function with external Codec.</li> <li>Supports slave modes, not master mode.</li> </ul>
SPI Interface	<ul style="list-style-type: none"> <li>Provides a duplex, synchronous and serial communication link with the peripheral devices.</li> <li>One SPI interface, only supports master mode.</li> <li>1.8 V operation voltage with clock rates up to 25 MHz.</li> </ul>
I2C Interface	<ul style="list-style-type: none"> <li>One I2C interface.</li> </ul>

<sup>1</sup> Optional.

	<ul style="list-style-type: none"> <li>● Comply with I2C-bus specification version.</li> </ul>
USB Interface	<ul style="list-style-type: none"> <li>● Compliant with USB 2.0 specification (slave mode only), with maximum transmission rate up to 480 Mbps.</li> <li>● Used for AT command communication, data transmission, software debugging, firmware upgrade.</li> <li>● USB Serial Driver: supports USB serial driver for Windows 7/8/8.1/10, Linux 2.6–5.12 and Android 4.x–11.x systems.</li> </ul>
UART Interfaces	<p><b>Main UART:</b></p> <ul style="list-style-type: none"> <li>● Used for AT command communication and data transmission.</li> <li>● Baud rates: up to 921600bps, 115200 bps by default.</li> <li>● Supports RTS and CTS hardware flow control.</li> </ul> <p><b>Debug UART:</b></p> <ul style="list-style-type: none"> <li>● Used for Linux console and log output.</li> <li>● Baud rate: 921600 bps.</li> <li>● Only use for debug UART, cannot use for universal UART.</li> </ul> <p><b>Auxiliary UART</b></p>
Network Indication	NET_STATUS to indicate network connectivity status.
AT Commands	Compliant with 3GPP TS 27.007, and 3GPP TS 27.005 and Quectel enhanced AT commands.
Antenna Interface	<ul style="list-style-type: none"> <li>● Main antenna interface (ANT_MAIN).</li> <li>● Bluetooth and Wi-Fi Scan antenna interface (ANT_BT/WIFI_SCAN).</li> <li>● 50 <math>\Omega</math> impedance.</li> </ul>
Transmitting Power	<ul style="list-style-type: none"> <li>● GSM850/EGSM900: Class 4 (33 dBm <math>\pm</math>2 dB).</li> <li>● DCS1800/PCS1900: Class 1 (30 dBm <math>\pm</math>2 dB).</li> <li>● LTE-FDD: Class 3 (23 dBm <math>\pm</math>2 dB).</li> </ul>
LTE Features	<ul style="list-style-type: none"> <li>● Supports up to Cat 1 FDD.</li> <li>● Supports 1.4/3/5/10/15/20 MHz RF bandwidth.</li> <li>● Supports uplink QPSK, 16QAM.</li> <li>● Supports downlink QPSK, 16QAM and 64QAM.</li> <li>● FDD: Max 10 Mbps (DL) / 5 Mbps (UL).</li> </ul>
GSM Features	<p><b>GPRS:</b></p> <ul style="list-style-type: none"> <li>● Supports GPRS multi-slot class 12.</li> <li>● Coding scheme: CS-1/CS-2/CS-3/CS-4.</li> <li>● Max 85.6 Kbps (DL) / 85.6 Kbps (UL).</li> </ul>
Internet Protocol Features	<ul style="list-style-type: none"> <li>● Supports TCP/UDP/PPP/NTP/NITZ/FTP/HTTP/PING/CMUX/HTTPS/FTPS/SSL/FILE/MQTT/MMS protocols.</li> <li>● Supports the protocols PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol).</li> </ul>
Firmware Upgrade	Use USB interface or FOTA to upgrade.

Temperature Range	<ul style="list-style-type: none"><li>● Operating Temperature Range: -35 °C to +75 °C <sup>2</sup>.</li><li>● Extended Operating Temperature Range: -40 °C to +85 °C <sup>3</sup>.</li><li>● Storage temperature range: -40 °C to +95 °C.</li></ul>
RoHS	All hardware components are fully compliant with EU RoHS directive.

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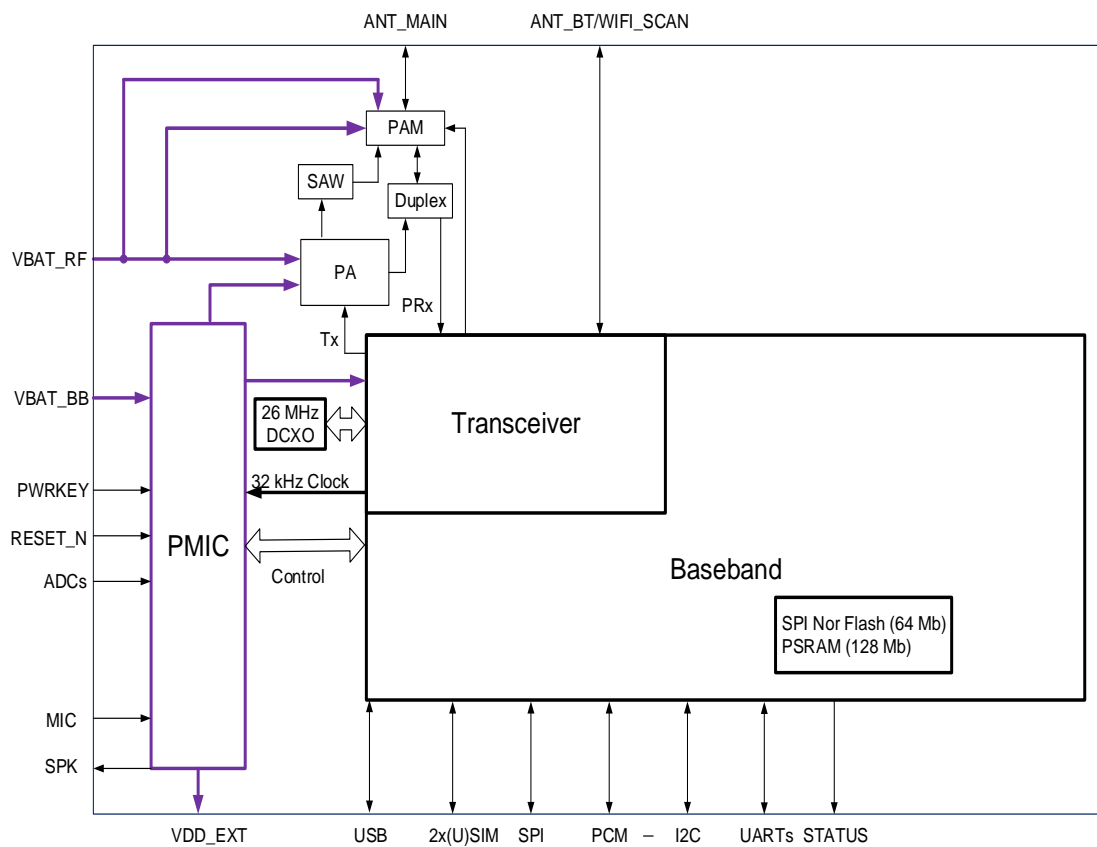
<sup>2</sup> Within operating temperature range, the module is 3GPP compliant.

<sup>3</sup> Within extended operating temperature range, proper mounting, heating sinks and active cooling may be required to make certain functions of the module such as voice, SMS, data transmission to be realized. Only one or more parameters like Pout might reduce in their value and exceed the specified tolerances. When the temperature returns to normal operating temperature levels, the module will meet 3GPP specifications again.

## 2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- Flash
- Radio frequency
- Peripheral interface



**Figure 1: EG915U-EU Functional Diagram**

## 2.4. Pin Assignment

The following figure illustrates the pin assignment of the module.

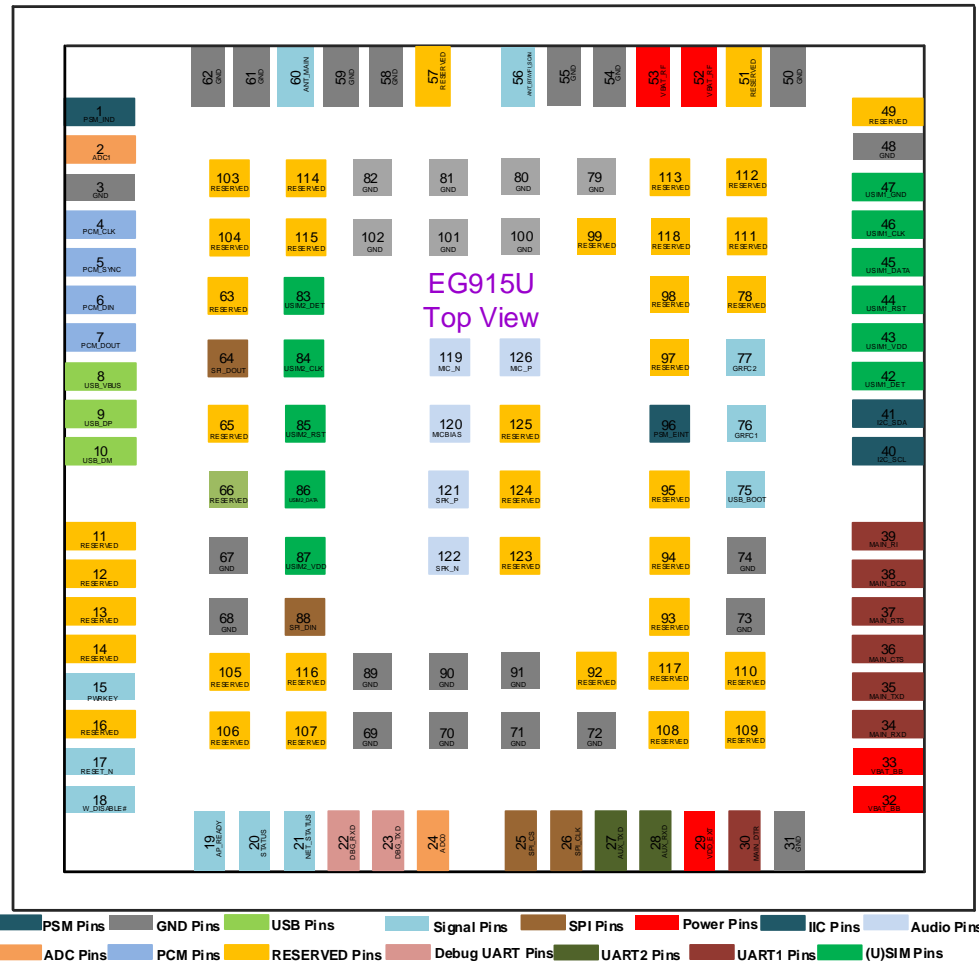


Figure 2: EG915U-EU Pin Assignment

### NOTE

1. USB\_BOOT cannot be pulled up before the module startup.
2. Keep NC and RESERVED pins unconnected, all GND pins shall be connected to the ground.
3. The functions of pin 1 is under development and we do not recommend using them.
4. EG915U series modules support dual SIM single stand by. For details, please contact Quectel Technical Support.



## 2.5. Pin Description

The following tables show the pin definition of EG915U-EU module.

**Table 5: I/O Parameters Definition**

Type	Description
AI	Analog Input
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

**Table 6: Pin Description**

Power Supply					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
VBAT_BB	32, 33	PI	Power supply for the module's baseband part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current up to 1 A
VBAT_RF	52, 53	PI	Power supply for the module's RF part		It must be provided with sufficient current up to 2.5 A
VDD_EXT	29	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V Iomax = 50 mA	Power supply for external GPIO's pull-up circuits. Add 2.2 $\mu$ F bypass capacitor when in use. If unused, keep this pin open.

## Turn On/Off

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PWRKEY	15	DI	Turn on/off the module	$V_{ILmax} = 0.5\text{ V}$	VBAT power domain.
RESET_N	17	DI	Reset the module		VBAT power domain. If unused, keep this pin open.

## Indication Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
STATUS	20	DO	Indicate the module's operation status	$V_{OHmin} = 1.35\text{ V}$ $V_{OLmax} = 0.45\text{ V}$	1.8 V power domain.
NET_STATUS	21	DO	Indicate the module's network activity status		If unused, keep this pin open.

## USB Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_VBUS	8	AI	USB connection detect	$V_{max} = 5.25\text{ V}$ $V_{min} = 3.5\text{ V}$ $V_{nom} = 5.0\text{ V}$	Typical: 5.0 V Minimum: 3.5 V If unused, keep this pin open.
USB_DP	9	AIO	USB differential data (+)		USB 2.0 compliant. Require differential impedance of 90 $\Omega$ . If unused, keep this pin open.
USB_DM	10	AIO	USB differential data (-)		

## (U)SIM Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USIM1_VDD	43	PO	(U)SIM1 card power supply	$I_{Omax} = 50\text{ mA}$ <b>For 1.8 V (U)SIM:</b> $V_{max} = 1.9\text{ V}$ $V_{min} = 1.7\text{ V}$ <b>For 3.0 V (U)SIM:</b> $V_{max} = 3.05\text{ V}$ $V_{min} = 2.7\text{ V}$	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_DATA	45	DIO	(U)SIM1 card data	<b>For 1.8 V (U)SIM:</b>	

				$V_{ILmax} = 0.6\text{ V}$ $V_{IHmin} = 1.26\text{ V}$ $V_{OLmax} = 0.45\text{ V}$ $V_{OHmin} = 1.35\text{ V}$ <b>For 3.0 V (U)SIM:</b> $V_{ILmax} = 1.0\text{ V}$ $V_{OHmin} = 1.95\text{ V}$ $V_{OLmax} = 0.45\text{ V}$ $V_{OHmin} = 2.55\text{ V}$	
USIM1_CLK	46	DO	(U)SIM1 card clock	<b>For 1.8 V (U)SIM:</b> $V_{OLmax} = 0.45\text{ V}$ $V_{OHmin} = 1.35\text{ V}$ <b>For 3.0 V (U)SIM:</b> $V_{OLmax} = 0.45\text{ V}$ $V_{OHmin} = 2.55\text{ V}$	
USIM1_RST	44	DO	(U)SIM1 card reset	<b>For 3.0 V (U)SIM:</b> $V_{OLmax} = 0.45\text{ V}$ $V_{OHmin} = 2.55\text{ V}$	
USIM1_DET	42	DI	(U)SIM1 card hot-plug detect	$V_{ILmin} = -0.3\text{ V}$ $V_{ILmax} = 0.6\text{ V}$ $V_{OHmin} = 1.26\text{ V}$ $V_{IHmax} = 2.0\text{ V}$	1.8 V power domain. If unused, keep this pin open.
USIM1_GND	47		Specified ground for (U)SIM1 card		Specified ground for (U)SIM1 card.
USIM2_VDD*	87	PO	(U)SIM2 card power supply	$I_{omax} = 50\text{ mA}$ <b>1.8 V (U)SIM:</b> $V_{max} = 1.9\text{ V}$ $V_{min} = 1.7\text{ V}$ <b>3.0 V (U)SIM:</b> $V_{max} = 3.05\text{ V}$ $V_{min} = 2.7\text{ V}$	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM2_DATA*	86	DIO	(U)SIM2 card data	<b>1.8 V (U)SIM:</b> $V_{ILmax} = 0.6\text{ V}$ $V_{OHmin} = 1.26\text{ V}$ $V_{OLmax} = 0.45\text{ V}$ $V_{OHmin} = 1.35\text{ V}$ <b>3.0 V (U)SIM:</b> $V_{ILmax} = 1.0\text{ V}$ $V_{OHmin} = 1.95\text{ V}$ $V_{OLmax} = 0.45\text{ V}$ $V_{OHmin} = 2.55\text{ V}$	
USIM2_CLK*	84	DO	(U)SIM2 card clock	<b>1.8 V (U)SIM:</b> $V_{OLmax} = 0.45\text{ V}$ $V_{OHmin} = 1.35\text{ V}$	
USIM2_RST*	85	DO	(U)SIM2 card reset	<b>3.0 V (U)SIM:</b> $V_{OLmax} = 0.45\text{ V}$	

				$V_{OHmin} = 2.55\text{ V}$	
USIM2_DET*	83	DI	(U)SIM2 card hot-plug detect	$V_{OHmin} = -0.3\text{ V}$ $V_{ILmax} = 0.6\text{ V}$ $V_{OHmin} = 1.26\text{ V}$ $V_{OLmax} = 2.0\text{ V}$	1.8 V power domain. If unused, keep this pin open.

#### Main UART Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
MAIN_CTS	36	DO	DTE clear to send signal to DCE (connect to DTE's CTS)	$V_{OLmax} = 0.45\text{ V}$ $V_{OHmin} = 1.35\text{ V}$	
MAIN_RTS	37	DI	DTE request to send signal to DCE (connect to DTE's RTS)	$V_{OHmin} = -0.3\text{ V}$ $V_{ILmax} = 0.6\text{ V}$ $V_{OHmin} = 1.26\text{ V}$ $V_{OLmax} = 2.0\text{ V}$	
MAIN_RXD	34	DI	Main UART receive		1.8 V power domain
MAIN_DCD	38	DO	Main UART data carrier detect		If unused, keep this pin open.
MAIN_TXD	35	DO	Main UART transmit	$V_{OLmax} = 0.45\text{ V}$ $V_{OHmin} = 1.35\text{ V}$	
MAIN_RI	39	DO	Main UART ring indication		
MAIN_DTR	30	DI	Main UART data terminal ready	$V_{OHmin} = -0.3\text{ V}$ $V_{ILmax} = 0.6\text{ V}$ $V_{OHmin} = 1.26\text{ V}$ $V_{OLmax} = 2.0\text{ V}$	

#### AUX UART Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
AUX_TXD	27	DO	Auxiliary UART transmit	$V_{OLmax} = 0.45\text{ V}$ $V_{OHmin} = 1.35\text{ V}$	
AUX_RXD	28	DI	Auxiliary UART receive	$V_{OHmin} = -0.3\text{ V}$ $V_{ILmax} = 0.6\text{ V}$ $V_{OHmin} = 1.26\text{ V}$ $V_{OLmax} = 2.0\text{ V}$	1.8 V power domain If unused, keep this pin open.

#### Debug UART Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
DBG_RxD	22	DI	Debug UART transmit	$V_{OHmin} = -0.3\text{ V}$ $V_{ILmax} = 0.6\text{ V}$	1.8 V power domain.

				$V_{OHmin} = 1.26\text{ V}$ $V_{OLmax} = 2.0\text{ V}$	If unused, keep this pin open.
DBG_TxD	23	DO	Debug UART receive	$V_{OLmax} = 0.45\text{ V}$ $V_{OHmin} = 1.35\text{ V}$	

#### I2C Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
I2C_SCL	40	OD	I2C serial clock		External pull-up resistor is required. 1.8 V only. If unused, keep this pin open.
I2C_SDA	41	OD	I2C serial data		If the I2C interface is used to connect to external codec, it cannot connect to other external devices.

#### PCM Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PCM_SYNC	5	DI	PCM data frame sync	$V_{OHmin} = -0.3\text{ V}$	1.8 V power domain. If unused, keep this pin open. Only support slave mode.
PCM_CLK	4	DI	PCM clock	$V_{ILmax} = 0.6\text{ V}$	
PCM_DIN	6	DI	PCM data input	$V_{OHmin} = 1.26\text{ V}$ $V_{OLmax} = 2.0\text{ V}$	
PCM_DOUT	7	DO	PCM data output	$V_{OLmax} = 0.45\text{ V}$ $V_{OHmin} = 1.35\text{ V}$	

#### RF Antenna Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ANT_MAIN	60	AIO	Main antenna interface		50 $\Omega$ impedance
ANT_BT/WIFI_SCAN	56	AIO	This RF interface includes both Bluetooth and Wi-Fi Scan function, which cannot be achieved simultaneously. Wi-Fi Scan can only receive but not transmit signal.		50 $\Omega$ impedance If unused, keep this pin open.

**GRFC Antenna Tuner Control Interface\***

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
GRFC1	76	DO	General RF Controller		If unused, keep this pin open.
GRFC2	77	DO			

**SPI Interface**

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SPI_CLK	26	DO	SPI clock	V <sub>OL</sub> max = 0.45 V V <sub>OH</sub> min = 1.35 V	Just master mode only.
SPI_CS	25	DO	SPI chip select		
SPI_DIN	88	DI	SPI master mode input	V <sub>IL</sub> min = -0.3 V V <sub>IL</sub> max = 0.6 V V <sub>IH</sub> min = 1.26 V V <sub>IH</sub> max = 2.0 V	
SPI_DOUT	64	DO	SPI master mode output	V <sub>OL</sub> max = 0.45V V <sub>OH</sub> min = 1.35V	

**ADC Interface**

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ADC0	24	AI	General-purpose ADC interface	Voltage range: 0 V to VBAT	If unused, keep this pin open.
ADC1	2	AI			

**Analog Audio Interfaces**

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
MIC_N	119	AI	Microphone analog input (-)	Vo = 2.2 V to 3.0 V Vnom = 2.2 V	
MICBIAS	120	PO	Bias voltage output for microphone		
SPK_P	121	AO	Analog audio differential output (+)		
SPK_N	122	AO	Analog audio differential output (-)		
MIC_P	126	AI	Microphone analog input (+)		

**GND Interfaces**

Pin Name	Pin No.
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67, 68, 69, 70, 71, 72, 73, 74, 79, 80, 81, 82, 89, 90, 91, 100, 101, 102

#### Other Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_BOOT	75	DI	Control pin for the module to enter download mode	$V_{ILmin} = -0.3\text{ V}$ $V_{ILmax} = 0.6\text{ V}$ $V_{IHmin} = 1.2\text{ V}$ $V_{IHmax} = 2.0\text{ V}$	1.8 V power domain. Active High A circuit that enables the module to enter the download mode must be reserved.
W_DISABLE#	18	DI	Airplane mode control	$V_{OHmin} = -0.3\text{ V}$ $V_{ILmax} = 0.6\text{ V}$ $V_{OHmin} = 1.26\text{ V}$ $V_{OLmax} = 2.0\text{ V}$	1.8 V power domain. Pulled up by default. When it is in low voltage level, the module can enter airplane mode. If unused, keep this pin open.
AP_READY	19	DI	Application processor ready		1.8 V power domain If unused, keep this pin open.
PSM_EINT*	96	DI	External interrupt pin; wake up the module from PSM.		If unused, keep this pin open.
PSM_IND*	1	DO	Indicate the module's power saving mode		

#### RESERVED Interfaces

Pin Name	Pin No.
RESERVED	11, 12, 13, 14, 16, 49, 51, 57, 63, 65, 66, 78, 92, 93, 94, 95, 97, 98, 99, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112, 113, 114, 115, 116, 117, 118, 123, 124, 125

## 2.6. EVB

In order to help customers to develop applications with the module conveniently, Quectel supplies an evaluation board (UMTS&LTE EVB), USB 2.0 data cable, earphone, antenna, and other peripherals to control or to test the module. For more details, please refer to **document [1]**.



# 3 Operating Characteristics

## 3.1. Operating Modes

The table below outlines operating modes of the module.

**Table 7: Overview of Operating Modes**

Mode	Details	
Normal Operation	Idle	Software is active. The module is registered on the network and ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	<b>AT+CFUN [=0]</b> command can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.	
Airplane Mode	<b>AT+CFUN [=4]</b> command or W_DISABLE# pin can set the module to airplane mode. In this case, RF function will be invalid.	
Sleep Mode	In this mode, current consumption of the module will be reduced to the minimal level, but the module can still receive paging, SMS, voice call and TCP/UDP data from network.	
Power Down Mode	In this mode, the VBAT power supply is constantly turned on and the software stops working.	

## 3.2. Sleep Mode

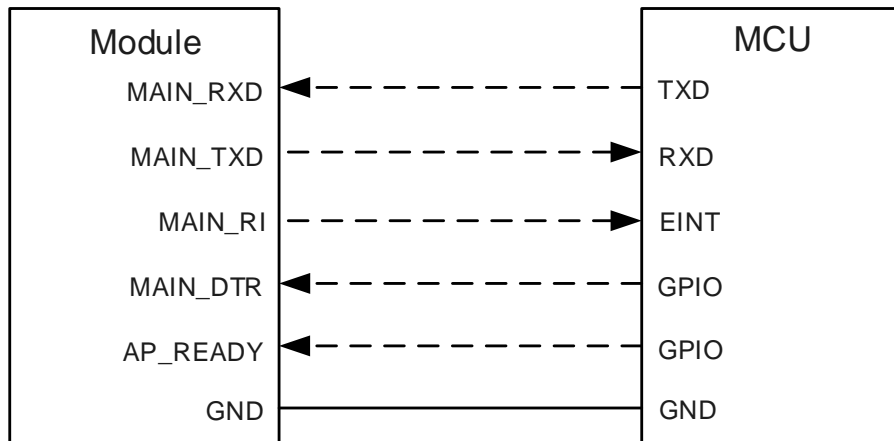
EG915U-EU is able to reduce its current consumption to an ultra-low value in the sleep mode. The following section describes power saving procedures of EG915U-EU module.

### 3.2.1. UART Application Scenario

If the host communicates with the module via UART interface, all the following two preconditions should be met to set the module enter into sleep mode:

- Execute **AT+QSClk=1** command to enable sleep mode.
- Ensure the MAIN\_DTR is held at a high level.

The following figure illustrates the connection between the module and the host.



**Figure 3: Sleep Mode Application via UART**

- Driving the host MAIN\_DTR low will wake up the module.
- When EG915U-EU has an URC to report, the URC will trigger the behavior of MAIN\_RI pin. Please refer to **Chapter 3.2.2** for details about MAIN\_RI behavior.

### 3.2.2. USB Application Scenario

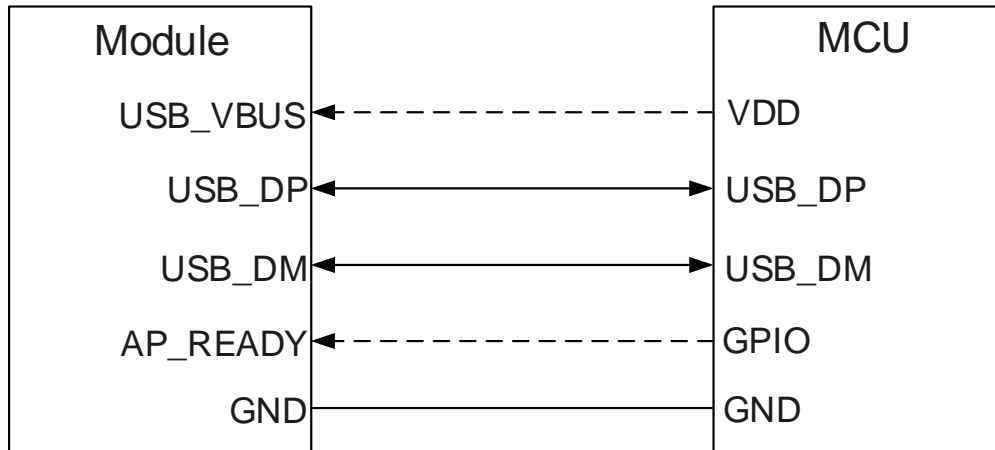
For the two situations below, three preconditions must be met to set the module enter sleep mode:

- Execute **AT+QSClk=1** command to enable sleep mode.
- Ensure the MAIN\_DTR is held at a high level or keep it open
- The host's USB Bus, which is connected with the module's USB interface, enters Suspend state.

### 3.2.2.1. USB Application with USB Remote Wakeup Function

The host supports USB Suspend/Resume and remote wakeup function.

The following figure illustrates the connection between the module and the host.



**Figure 4: Sleep Mode Application with USB Remote Wakeup**

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module will send remote wake-up signals to USB Bus to wake up the host.

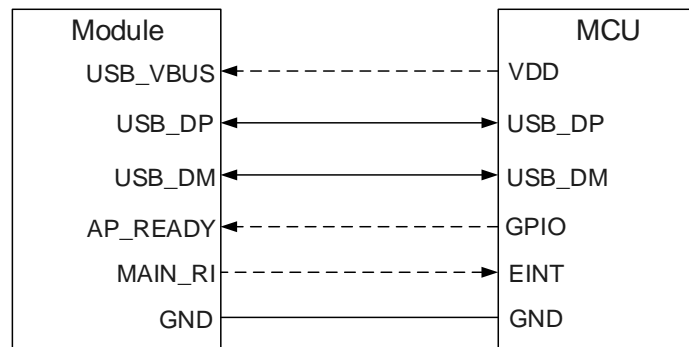
#### NOTE

Pay attention to the level match shown in dotted line between the module and the host.

### 3.2.2.2. USB Application with USB Suspend/Resume and MAIN\_RI Function

If the host supports USB Suspend/Resume, but does not support remote wakeup function, the MAIN\_RI signal is needed to wake up the host.

The following figure illustrates the connection between the module and the host.



**Figure 5: Sleep Mode Application with RI**

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, MAIN\_RI signal will wake up the host.

#### NOTE

USB suspend is supported on Linux system but not supported on Windows system.

## 3.3. Airplane Mode

When the module enters into airplane mode, the RF function will be disabled, and all AT commands related to the RF function are inaccessible. You can set this mode via the following ways.

### 3.3.1. Hardware

The W\_DISABLE# pin is pulled up by default. Its control function for airplane mode is disabled by default and **AT+QCFG="airplanecontrol",1** can be used to enable the function. Driving it low will set the module enter airplane mode.

### 3.3.2. Software

**AT+CFUN=<fun>** command provides choices of the functionality level through setting <fun> into 0, 1 or 4.

- **AT+CFUN=0**: Minimum functionality (disable RF function and (U)SIM function).
- **AT+CFUN=1**: Full functionality (default).
- **AT+CFUN=4**: Airplane mode (disable RF function).

## 3.4. Power Supply

### 3.4.1. Power Supply Pins

EG915U-EU provides 4 VBAT pins for connection with an external power supply.

- Two VBAT\_RF pins for RF part.
- Two VBAT\_BB pins for BB part.

**Table 8: Pin Definition of Power Supply**

Pin Name	Pin No.	I/O	Description	Comment
VBAT_BB	32, 33	PI	Power supply for the module's baseband part	
VBAT_RF	52, 53	PI	Power supply for the module's RF part	
VDD_EXT	29	PO	Provide 1.8 V for external circuit	Power supply for external GPIO's pull-up circuits. Add 2.2 $\mu$ F bypass capacitor when in use. If unused, keep this pin open.

### 3.4.2. Reference Design for Power Supply

The power design for the module is very important, as the performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current of 3.0 A at least. If the voltage drops between input and output is not too high, it is suggested that an LDO should be used to supply power to the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is recommended.

The following figure illustrates a reference design for +5 V input power source. The typical output of the power supply is about 3.8 V and the maximum load current is 3.0 A.

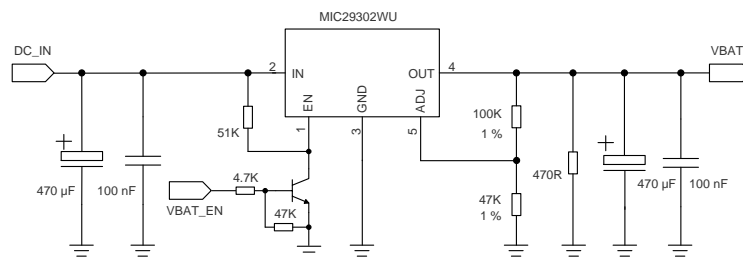


Figure 6: Reference Design of Power Supply

### 3.4.3. Requirements for Voltage Stability

The power supply range of the module is from 3.3 V to 4.3 V. Please make sure the input voltage will never drop below 3.3 V.

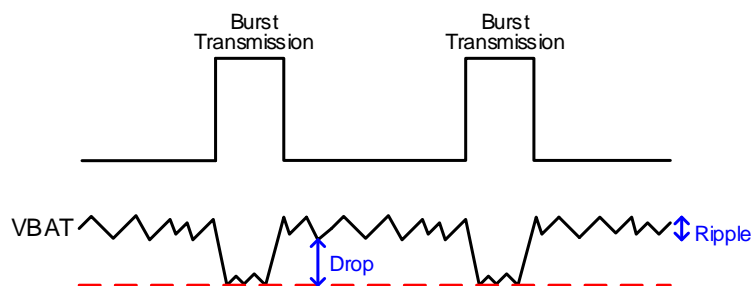
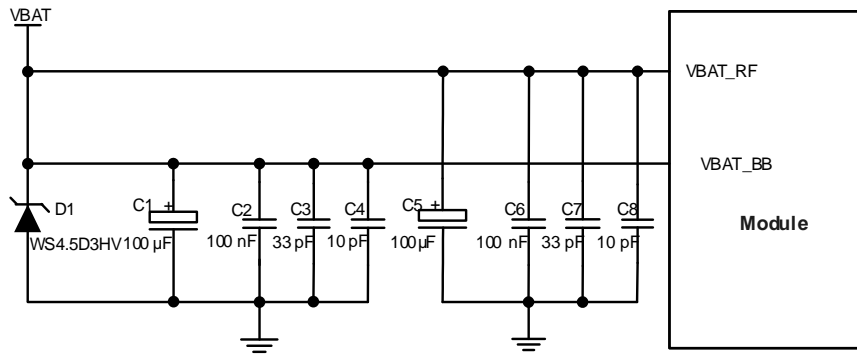


Figure 7: Power Supply Limits during Burst Transmission

To decrease voltage 's drop, a bypass capacitor of about 100 µF with low ESR (ESR = 0.7 Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors for composing the MLCC array, and place these capacitors close to VBAT pins. The main power supply from an external application must be a single voltage source and can be expanded to two sub paths with the star structure. The width of VBAT\_BB trace should be no less than 2.0 mm. The width of VBAT\_RF trace should be no less than 2.5 mm. In principle,

the longer the VBAT trace is, the wider it will be.

In addition, in order to ensure the stability of power source, it is suggested that a WS4.5D3HV TVS diode of which reverse stand-off voltage is 4.7 V and peak pulse power is up to 2550 W should be used. Reference circuit is shown as below:



**Figure 8: Star Structure of the Power Supply**

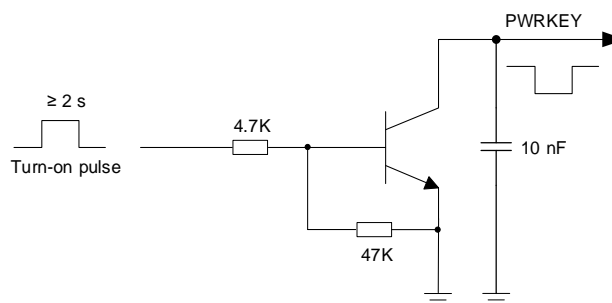
## 3.5. Turn On

### 3.5.1. Turn on the Module with PWRKEY

**Table 9: Pin Definition of PWRKEY**

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	15	DI	Turn on/off the module	VBAT power domain.

When the module is in power off mode, it can be turned on and enter normal operation mode by driving the PWRKEY low for at least 2 s. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.



**Figure 9: Reference Circuit of Turing on the Module with Driving Circuit**

Another way to control the PWRKEY is using a button directly. A TVS component is indispensable to be placed nearby the button for ESD protection.

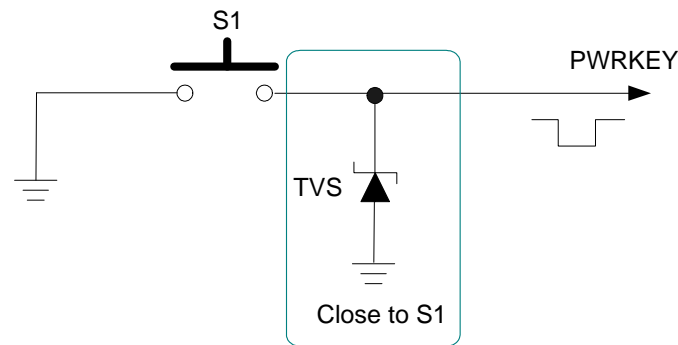


Figure 10: Reference Circuit of Turing on the Module with Keystroke

The turn on scenario is illustrated in the following figure.

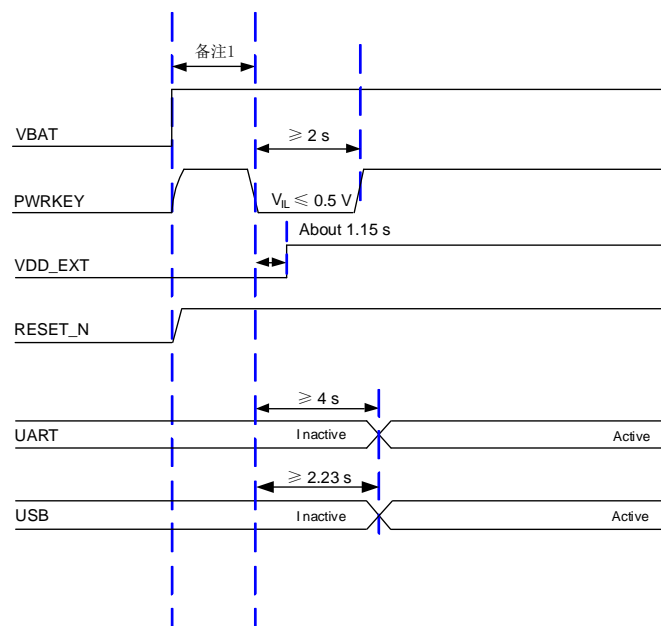


Figure 11: Power-on Timing

**NOTE**

1. Please make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is no less than 30 ms.
2. PWRKEY can be pulled down directly to GND with a recommended 1 kΩ resistor if module needs to be powered on automatically and shutdown is not needed.



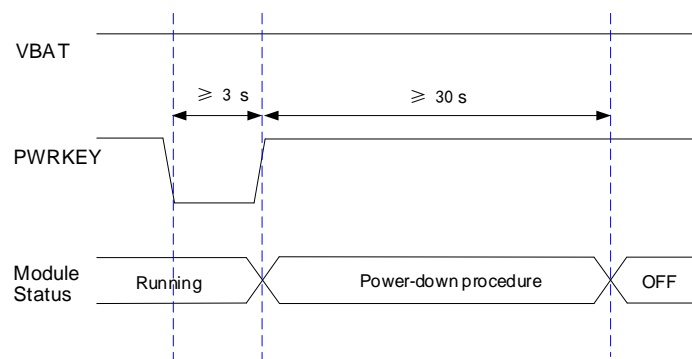
## 3.6. Turn Off

The following procedures can be used to turn off the module:

- Using the PWRKEY pin.
- Using **AT+QPOWD** command.

### 3.6.1. Turn off the Module with PWRKEY

Driving the PWRKEY to a low-level voltage for at least 3 s, then the module will execute power-down procedure after the PWRKEY is released. The turn off scenario is illustrated in the following figure.



**Figure 12: Power-down Timing**

### 3.6.2. Turn off the Module with AT Command

It is safe to use AT+QPOWD command to turn off the module, which is equal to turn off the module via PWRKEY Pin.

Please refer to **document [2]** for details about **AT+QPOWD** command.

#### NOTE

1. To avoid damaging internal flash, do not switch off the power supply when the module works normally. Only after shutting down the module with PWRKEY or AT command can you cut off the power supply.
2. When keeping the PWRKEY to the ground and the AT command cannot be used to turn off, the module can only be forced to turn off by cutting off the VBAT power supply. Therefore, we recommend that you can turn on or turn off the module by pulling up and pulling down the PWEKEY

instead of keeping the PWRKEY to the ground.

3. The time for the module to log out of the network is related to the current network status, so the specific shutdown time is related to the network status, please pay attention to the shutdown time in the design.

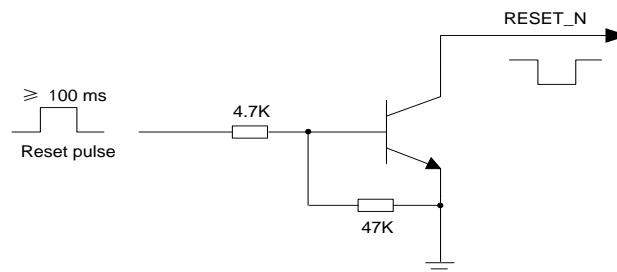
### 3.7. Reset

The module can be reset by driving the RESET\_N low for at least 100 ms and then releasing it. The RESET\_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

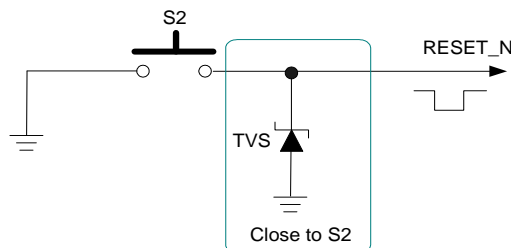
**Table 10: Pin Definition of RESET**

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	17	DI	Reset the module	VBAT power domain. Active low. If unused, keep this pin open.

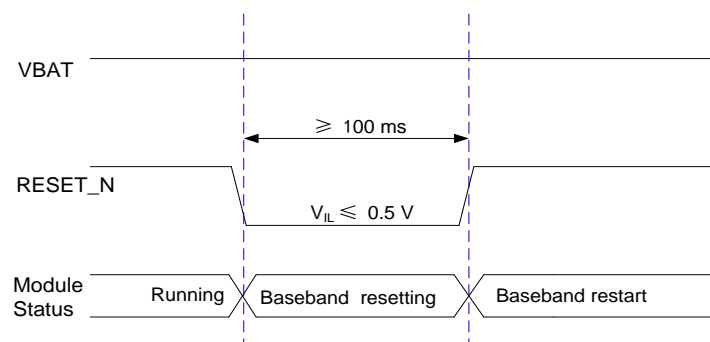
The recommended circuit is equal to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET\_N.



**Figure 13: Reference Circuit of RESET\_N with Driving Circuit**



**Figure 14: Reference Circuit of RESET\_N with Button**



**Figure 15: Reset Timing**

**NOTE**

1. Please ensure that there is no capacitance with the value exceeding 10 nF on PWRKEY and RESET\_N pins.
2. It is recommended to use RESET\_N only when failing to turn off the module by **AT+QPOWD** command or PWRKEY pin.

# 4 Application Interfaces

## 4.1. Analog Audio Interfaces

The module provides 1 analog audio input channel and 1 analog audio output channel. The pin definition is shown below:

**Table 11: Pin Definition of Audio Interfaces**

Pin Name	Pin No.	I/O	Description
MIC_N	119	AI	Microphone analog input (-)
MICBIAS	120	PO	Bias voltage output for microphone
SPK_P	121	AO	Analog audio differential output (+)
SPK_N	122	AO	Analog audio differential output (-)
MIC_P	126	AI	Microphone analog input (+)

- AI channels are differential output channels, which can be applied for input of microphone. (usually an electret microphone is used).
- AO channels are differential output channels, which can be applied for output receiver.

### 4.1.1. Audio Interfaces Design

It is recommended to use the electret microphone with dual built-in capacitors (e.g. 10 pF and 33 pF) for filtering out RF interference, thus reducing TDD noise. The 33 pF capacitors are used for filtering interference of EGSM900. Without placing this capacitor, TDD noise could be heard. The 10 pF capacitor here is used for filtering out RF interference at DCS1800. Please note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, customers would have to discuss with their capacitor vendors to choose the most suitable capacitor for filtering out high-frequency noises.

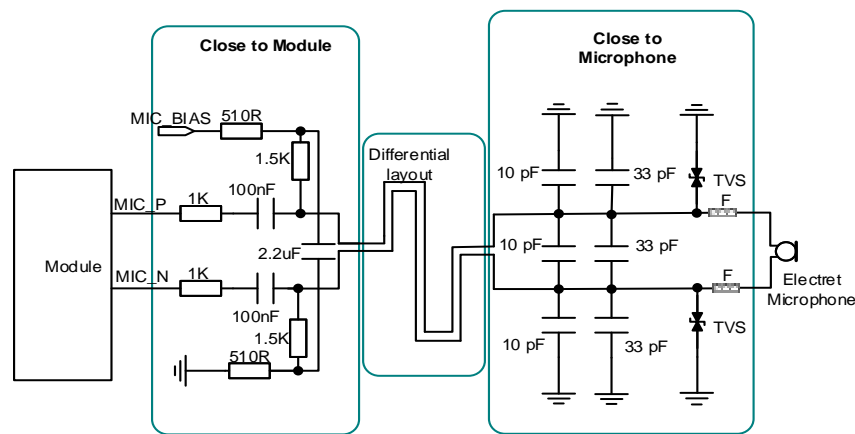
The filter capacitors on the PCB board should be placed as close to the audio devices or audio interfaces as possible, and the traces should be as short as possible. they should go through the filter capacitors before arriving other connection points.

In order to reduce radio or other signal interference, the radio frequency antenna should be far away from the audio interface and audio traces. The power traces should not be parallel to the audio traces, and should be far away from the audio traces.

The differential audio traces must be routed according to the differential signal layout rule.

#### 4.1.2. Microphone Interface Design

The microphone channel reference circuit is shown in the following figure.



**Figure 16: Reference Design for Microphone Interface**

#### NOTE

MIC channel is sensitive to ESD, so it is not recommended to remove the ESD components used for protecting the MIC.

### 4.1.3. Receiver Interface Design

The receiver channel reference circuit is shown in the following figure:

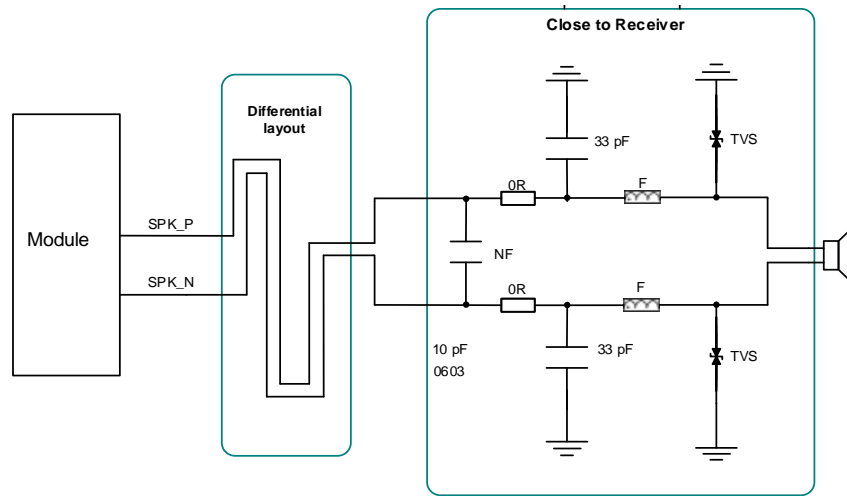


Figure 17: Reference Design for Receiver Interface

## 4.2. USB Interface

EG915U-EU provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports full-speed (12 Mbps) and high-speed (480 Mbps) modes. The USB interface can only serve as a slave device and is used for AT command communication, data transmission, software debugging and firmware upgrade.

Table 12: Functions of the USB Interface

Functions	
Data communication with external AP	Y
AT command communication	Y
Data transmission	Y
GNSS NMEA output	N
Software debugging	Y
Firmware upgrade	Y

Voice over USB

N

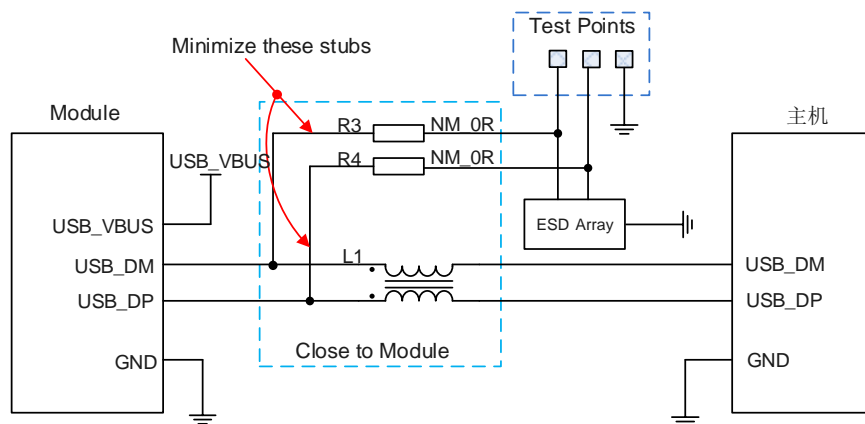
Pin definition of the USB interface is here as follows:

**Table 13: Pin Definition of USB Interface**

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	8	AI	USB connection detect	Typical 5.0 V Minimum 3.5 V
USB_DP	9	AIO	USB differential data (+)	USB 2.0 compliant. Require differential impedance of 90 $\Omega$ . If unused, keep this pin open.
USB_DM	10	AIO	USB differential data (-)	

For more details about the USB 2.0 specifications, please visit <http://www.usb.org/home>.

It is recommended to reserve test points for debugging and firmware upgrading in customers' designs. The following figure shows a reference circuit of USB interface.



**Figure 18: Reference Circuit of USB Application**

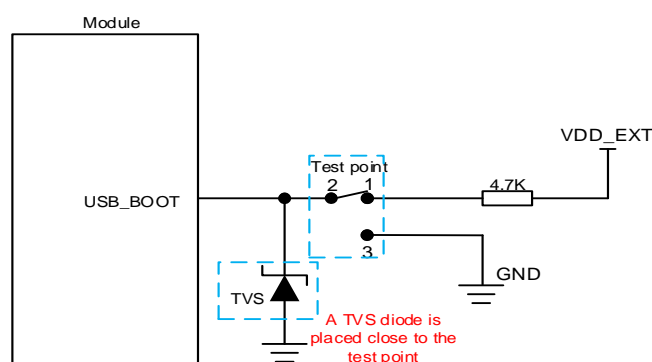
A common mode choke L1 is recommended to be added in series between the module and customer's MCU in order to suppress EMI spurious transmission. Meanwhile, the 0  $\Omega$  resistors (R3 and R4) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. In order to ensure the integrity of USB data line signal, L1, R3 and R4 components must be placed close to the module, and also resistors R3 and R4 should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles should be complied with when designing the USB interface, to meet USB specifications.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90  $\Omega$ .
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces.
- Please pay attention to the selection of the ESD component on the USB data line. Its parasitic capacitance should not exceed 2 pF and should be placed as close as possible to the USB interface.

### 4.3. USB\_BOOT Interface

The module provides a USB\_BOOT pin. You can pull up USB\_BOOT to VDD\_EXT before powering up, and the module will enter download mode when it is powered on. In this mode, the module supports firmware upgrade over USB interface.



**Figure 19: Reference Circuit of USB\_BOOT Interface**

#### NOTE

Please make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is no less than 30 ms.



## 4.4. (U)SIM Interface

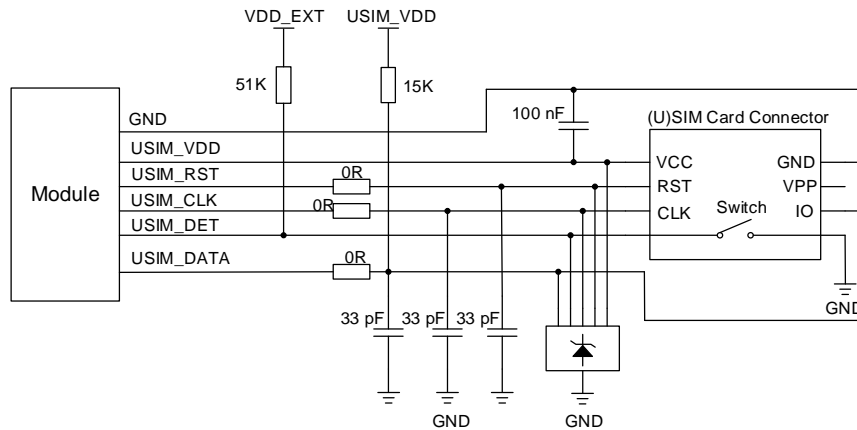
EG915U-EU provides 2 (U)SIM interfaces, dual SIM single stand by. The (U)SIM interface circuitry meets ETSI requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported.

**Table 14: Pin Definition of (U)SIM Interface**

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	43	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_DATA	45	DIO	(U)SIM1 card data	
USIM1_CLK	46	DO	(U)SIM1 card clock	
USIM1_RST	44	DO	(U)SIM1 card reset	
USIM1_DET	42	DI	(U)SIM1 card hot-plug detect	1.8 V power domain If unused, keep this pin open.
USIM1_GND	47		Specified ground for (U)SIM1 card	Specified ground for (U)SIM1 card
USIM2_VDD*	87	PO	(U)SIM2 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM2_DATA*	86	DIO	(U)SIM2 card data	
USIM2_CLK*	84	DO	(U)SIM2 card clock	
USIM2_RST*	85	DO	(U)SIM2 card reset	
USIM2_DET*	83	DI	(U)SIM2 card hot-plug detect	1.8 V power domain If unused, keep this pin open.

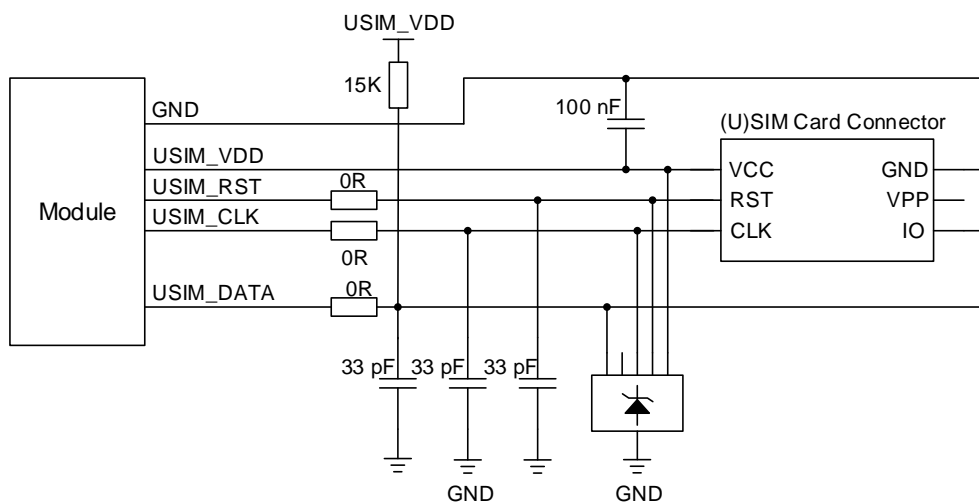
The module supports (U)SIM card hot-plug via the USIM\_DET pin, and both high- and low-level detections are supported. By default, it is disabled, and can be configured via **AT+QSIMDET** command. Please refer to **document [2]** for details about the command.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.



**Figure 20: Reference Circuit of (U)SIM Interface with an 8-Pin (U)SIM Card Connector**

If (U)SIM card detection function is not needed, please keep USIM\_DET disconnected. A reference circuit for (U)SIM card interface with a 6-pin (U)SIM card connector is illustrated in the following figure.



**Figure 21: Reference Circuit of (U)SIM Interface with a 6-Pin (U)SIM Card Connector**

In order to enhance the reliability and availability of the (U)SIM card in applications, please follow the criteria below in (U)SIM circuit design.

- Keep placement of (U)SIM card connector as close to the module as possible. Keep the trace length as less than 200 mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Keep the trace width of ground and USIM\_VDD no less than 0.5 mm to maintain the same electric potential.
- To avoid cross-talk between USIM\_DATA and USIM\_CLK, keep them away from each other and shield them with surrounded ground.

- In order to offer good ESD protection, it is recommended to add a TVS diode array whose parasitic capacitance should not be more than 15 pF. The 0  $\Omega$  resistors should be added in series between the module and the (U)SIM card to facilitate debugging. Add 33 pF capacitors parallel on USIM\_DATA, USIM\_CLK and USIM\_RST signal lines to filter RF interference of EGSM900. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM\_DATA can improve anti-jamming capability of the (U)SIM card. If the (U)SIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor near the (U)SIM card connector.

**NOTE**

EG915U series modules support dual SIM single stand by. For details, please contact Quectel Technical Support.

## 4.5. I2C and PCM Interfaces

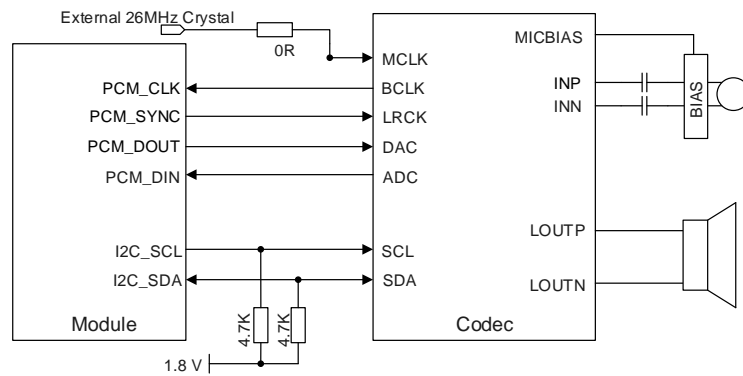
EG915U-EU provides one I2C interface and one Pulse Code Modulation (PCM) interface.

The PCM interface of EG91U-EU series only supports slave mode, not master mode. Therefore, an external clock must to be provided to the Codec. The following table shows the pin definition I2C of and PCM interfaces which can be applied on audio.

**Table 15: Pin Definition of I2C and PCM Interface**

Pin Name	Pin No.	I/O	Description	Comment
I2C_SCL	40	OD	I2C serial clock	External pull-up resistor is required. 1.8 V only. If unused, keep this pin open. If the I2C interface is used to connect to external codec, it cannot connect to other external devices.
I2C_SDA	41	OD	I2C serial data	
PCM_DIN	6	DI	PCM data input	
PCM_DOUT	7	DO	PWM data output	
PCM_SYNC	5	DI	PCM data frame sync	
PCM_CLK	4	DI	PCM clock	

The following figure shows a reference design of PCM interface with external Codec IC.



**Figure 22: Reference Circuit of PCM Application with Audio Codec**

## 4.6. UART Interfaces

The module provides 3 UART interfaces and the following shows their features:

- The main UART interface supports 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps and 921600 bps baud rates, the default is 115200 bps. This interface is used for data transmission and AT command communication. Supports RTS and CTS hardware flow control.
- The debug UART interface supports 921600 bps baud rate. It is used for the output of partial logs.
- Auxiliary UART.

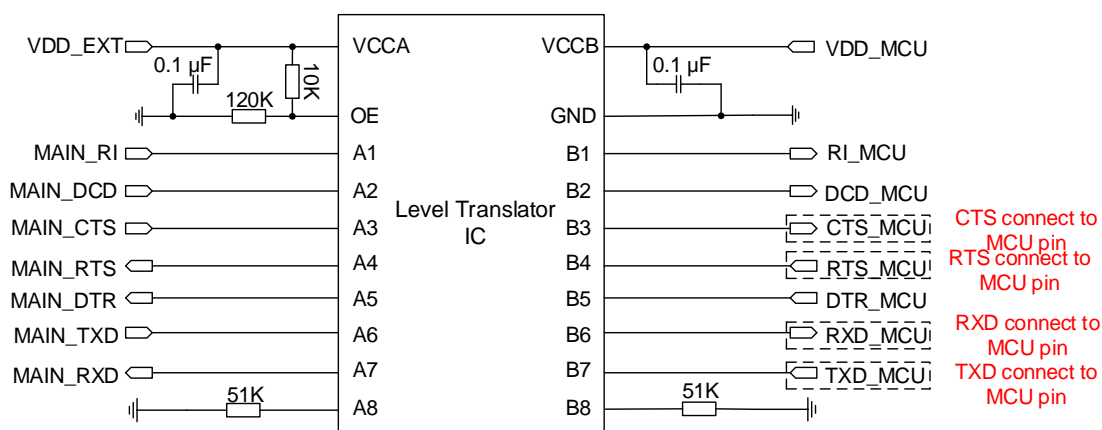
The following tables show the pin definition of main UART interface.

**Table 16: Pin Definition of UART Interface**

Pin Name	Pin No.	I/O	Description	Comment
MAIN_CTS	36	DO	DTE clear to send signal to DCE (connect to DTE's CTS)	
MAIN_RTS	37	DI	DTE request to send signal to DCE (connect to DTE's RTS)	
MAIN_RXD	34	DI	Main UART receive	1.8 V power domain
MAIN_DCD	38	DO	Main UART data carrier detect	
MAIN_TXD	35	DO	Main UART transmit	

MAIN_RI	39	DO	Main UART ring indication	
MAIN_DTR	30	DI	Main UART data terminal ready	
AUX_TXD	27	DO	Auxiliary UART transmit	
AUX_RXD	28	DI	Auxiliary UART receive	
DBG_RxD	22	DI	Debug UART transmit	1.8 V power domain If unused, keep this pin open.
DBG_TxD	23	DO	Debug UART receive	

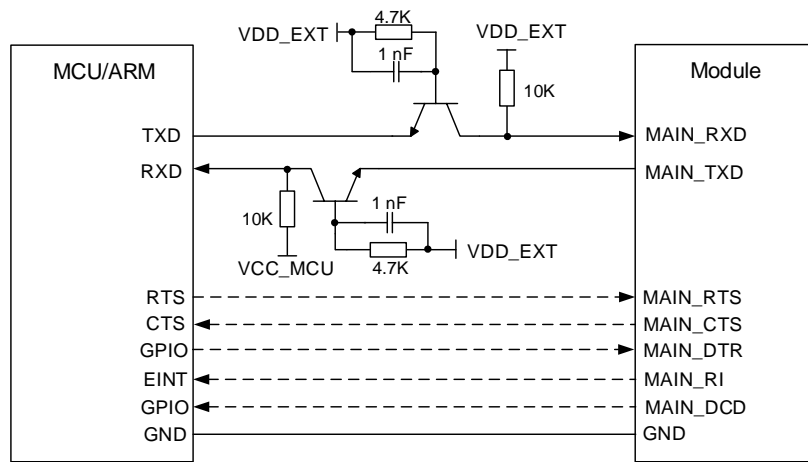
The module provides 1.8 V UART interfaces. A level translator should be used if the application is equipped with a 3.3 V UART interface. A level translator TXS0108EPWR provided by Texas Instruments is recommended. The following figure shows a reference design.



**Figure 23: Reference Circuit with Translator Chip**

Please visit <http://www.ti.com> for more information.

Another example with transistor translation circuit is shown as below. For the design of circuits in dotted lines, please refer to that of the circuits in solid lines, but please pay attention to the direction of connection.



**Figure 24: Reference Circuit with Transistor Circuit**

**NOTE**

1. Transistor circuit solution is not suitable for applications with baud rates exceeding 460 kbps.
2. Module's CTS connect to MCU's CTS, module's RTS connect to MCU's RTS. In addition, pay attention to UART's CTS and RTS input and output directions.

## 4.7. ADC Interface

The module provides 2 Analog-to-Digital Converter (ADC) interface.

- **AT+QADC=0** can be used to read the voltage value on ADC0 pin.
- **AT+QADC=1** can be used to read the voltage value on ADC1 pin.

For more details about these AT commands, please refer to **document [2]**.

In order to improve the accuracy of ADC, the trace of ADC should be surrounded by ground.

Table 17: Pin Definition of ADC

Pin Name	Pin No.	I/O	Description	Note
ADC0	24	AI	General-purpose ADC interface	1 kΩ resistor must be connected in series when using. If unused, keep this pin open.
ADC1	2	AI		

Table 18: Characteristics of ADC Interface

Name	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0	-	VBAT	V
ADC1 Voltage Range	0	-	VBAT	V
ADC Resolution	-	12	-	bits

#### NOTE

1. The input voltage of ADC should not exceed its corresponding voltage range.
2. It is recommended to use resistor divider circuit for ADC application.
3. If input voltage of ADC interface is designed with a resistor divider circuit, the resistance value of the external divider resistor must be less than 100 kΩ, otherwise the measurement accuracy of the ADC will be reduced significantly.

## 4.8. SPI Interface

The SPI interface of the EG915U-EU module only supports the master mode. It communicates with peripherals in a synchronous duplex serial manner. It has a working voltage of 1.8 V and a maximum clock frequency of 25 MHz.

Table 19: Pin Definition of SPI Interface

Pin Name	Pin No.	I/O	Description	Note
SPI_CLK	26	DO	SPI clock	

SPI_CS	25	DO	SPI chip select	Just master mode only.
SPI_DIN	88	DI	SPI master mode input	
SPI_DOUT	64	DO	SPI master mode output	

#### NOTE

When the universal 4-wire SPI interface is used to connect Nor Flash, it supports Flash basic reading, writing, erasing etc. It needs to perform erasing and writing balanced protection by itself. It does not support the file system and can only be stored.

## 4.9. Control Signal

Relative interfaces' pin descriptions are here as follows:

**Table 20: Pin Definition of Control Signal**

Pin Name	Pin No.	I/O	Description	Comment
W_DISABLE#	18	DI	Airplane mode control	1.8 V power domain Pulled up by default. When it is in low voltage level, the module can enter airplane mode. If unused, keep this pin open.

### 4.9.1. W\_DISABLE#

The module provides a W\_DISABLE# pin to enable or disable airplane mode through hardware operation. W\_DISABLE# is pulled up by default, and driving it low will set the module to airplane mode. Its control function for airplane mode is disabled by default and **AT+QCFG= "airplanecontrol", 1** can be used to enable the function.

**AT+CFUN=<fun>** command provides the choice of the functionality level through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality mode (RF functions are disabled).
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** RF function is disabled (Airplane mode).



## 4.10. Indication Signal

Relative interfaces' pin descriptions are here as follows:

**Table 21: Pin Definition of Indication Signal**

Pin Name	Pin No.	I/O	Description	Note
STATUS	20	DO	Indicate the module's operation status	1.8 V power domain If unused, keep this pin open.
AP_READY	19	DI	Application processor ready	1.8 V power domain If unused, keep this pin open.
NET_STATUS	21	DO	Indicate the module's network activity status	

### 4.10.1. Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The module provides two network indication pins: NET\_MODE and NET\_STATUS. The following tables describe pin definition and logic level changes in different network status.

**Table 22: Working State of the Network Connection Status/Activity Indication**

Pin Name	Status	Description
NET_STATUS	Flicker slowly (200 ms High/1800 ms Low)	Network searching
	Flicker quickly (234 ms High/266 ms Low)	Idle
	Flicker quickly (63 ms Low/62 ms High)	Data transfer is ongoing
	Always high	Voice calling

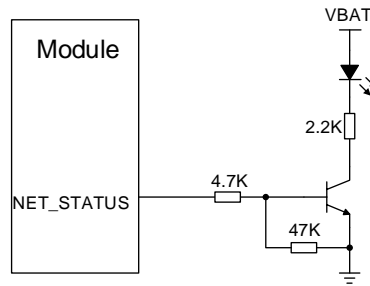


Figure 25: Reference Circuit of the Network Status Indication

#### 4.10.2. STATUS

The STATUS pin is an open drain output for indicating the module's operation status. It will output high level when module is powered ON successfully. Otherwise, STATUS will output low level.

A reference circuit is shown as below.

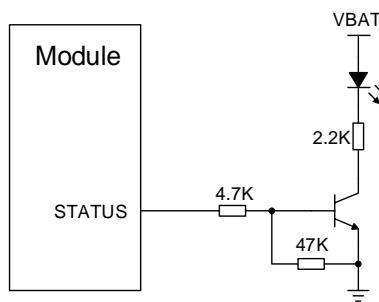


Figure 26: Reference Circuits of STATUS

#### 4.10.3. MAIN\_RI

**AT+QCFG= "risignalttype", "physical"** command can be used to configure MAIN\_RI behavior. No matter on which port a URC is presented, the URC will trigger the behavior of MAIN\_RI.

#### NOTE

The URC can be outputted via UART port, USB AT port and USB modem port, which can be set by **AT+QURCCFG** command. The default port is USB AT port.

In addition, MAIN\_RI behaviors can be configured flexibly. The default behavior of the MAIN\_RI is shown as below.

**Table 23: Behaviors of the MAIN\_RI**

State	Response
Idle	MAIN_RI keeps at high level
URC	MAIN_RI outputs 120 ms low pulse when a new URC return.

The MAIN\_RI behavior can be changed via **AT+QCFG="urc/ri/ring"**<sup>\*</sup>. Please refer to **document [2]** for details.

# 5 RF Specifications

## 5.1. Cellular Network

### 5.1.1. Antenna Interface & Frequency Bands

The pin definition is shown below:

**Table 24: Pin Definition of Cellular Network Interface**

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	AIO	Main antenna interface	50 $\Omega$ impedance.
ANT_BT/WIFI_SCAN	56	AIO	This RF interface includes both Bluetooth and Wi-Fi Scan function, which cannot be achieved simultaneously. Wi-Fi Scan can only receive but not transmit signal.	

#### NOTE

Only passive antennas are supported.

**Table 25: Operating Frequency of EG915U-EU**

Operating Frequency	Transmit (MHz)	Receive (MHz)
GSM850	824-849	869-894
PCS1900	1850-1910	1930-1990
EGSM900	880-915	925-960

DCS1800	1710-1785	1805-1880
LTE-B1	1920-1980	2110-2170
LTE-B3	1710-1785	1805-1880
LTE-B5	824-849	869-894
LTE-B7	2500-2570	2620-2690
LTE-B8	880-915	925-960
LTE-B20	832-862	791-821
LTE-B28	703-748	758-803

### 5.1.2. Tx Power

The following table shows the RF output power of the module.

**Table 26: Tx Power**

Frequency	Max. RF Output Power	Min. RF Output Power
GSM850/EGSM900	33 dBm $\pm$ 2 dB	5 dBm $\pm$ 5 dB
DCS1800/PCS1900	30 dBm $\pm$ 2 dB	0 dBm $\pm$ 5 dB
LTE-FDD B1/B3/B5/B7/B8/B20/B28	23 dBm $\pm$ 2 dB	< -39 dBm

#### NOTE

In GPRS 4 slots Tx mode, the maximum output power is reduced by 6 dB. The design conforms to the GSM specification as described in **Chapter 13.16** of 3GPP TS 51.010-1.

### 5.1.3. Receiving Sensitivity

The following table shows conducted RF receiving sensitivity of the module.

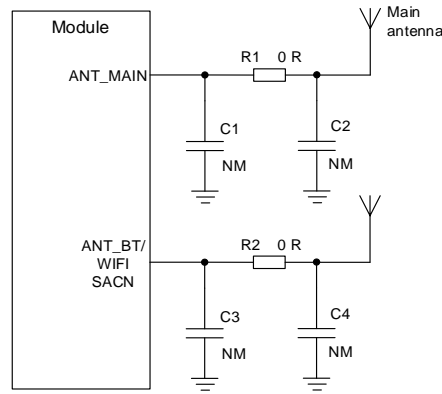
**Table 27: Conducted RF Receiving Sensitivity of EG915U-EU**

Frequency	Receiving Sensitivity (Typ.)	3GPP Requirement (SIMO) Primary+ Diversity
	Primary	
GSM850	-108	-102 dBm
EGSM900	-106.5	-102 dBm
DCS1800	-107.5	-102 dBm
PCS1900	-107	-102 dBm
LTE-FDD B1 (10 MHz)	-97	-96.3 dBm
LTE-FDD B3 (10 MHz)	-98.8	-96.3 dBm
LTE-FDD B5 (10 MHz)	-97.4	-94.3 dBm
LTE-FDD B7 (10 MHz)	-96.1	-94.3 dBm
LTE-FDD B8 (10 MHz)	-97.5	-93.3 dBm
LTE-FDD B20 (10 MHz)	-98.9	-93.3 dBm
LTE-FDD B28 (10 MHz)	-99.4	-94.8 dBm

### 5.1.4. Reference Design

The module provides 2 RF antenna interfaces for antenna connection.

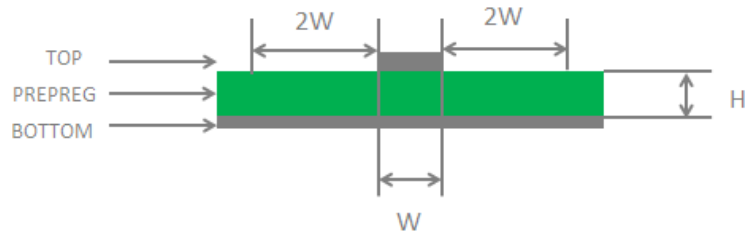
It is recommended to reserve a  $\Pi$ -type matching circuit for better RF performance, and the  $\Pi$ -type matching components (R1, C1, C2 and R2, C3, C4) should be placed as close to the antenna as possible. The capacitors are not mounted by default.



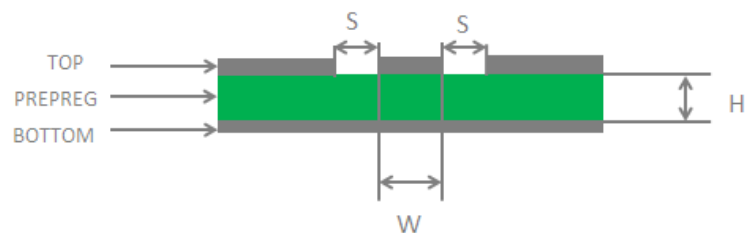
**Figure 27: Reference Circuit for RF Antenna Interfaces**

## 5.2. Reference Design of RF Routing

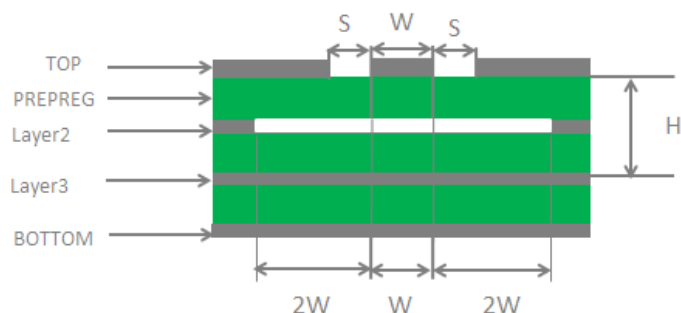
For user's PCB, the characteristic impedance of all RF traces should be controlled to  $50\ \Omega$ . The impedance of the RF traces is usually determined by the trace width ( $W$ ), the materials' dielectric constant, height from the reference ground to the signal layer ( $H$ ), and the space between RF traces and grounds ( $S$ ). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.



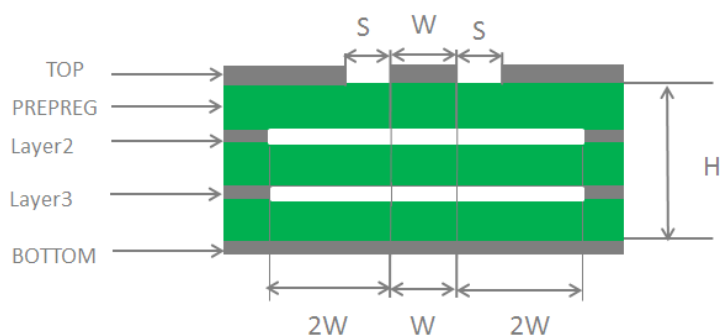
**Figure 28: Microstrip Design on a 2-layer PCB**



**Figure 29: Coplanar Waveguide Design on a 2-layer PCB**



**Figure 30: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)**



**Figure 31: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)**

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50  $\Omega$ .
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- Keep the reference ground of RF traces complete. Meanwhile, add some ground vias around RF traces and the reference ground to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces ( $2 \times W$ ). Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, please refer to **document [3]**.



### 5.3. Requirements for Antenna Design

Table 28: Requirements for Antenna Design

Antenna Type	Requirements
GSM/LTE	VSWR: $\leq 2$
	Efficiency: $> 30\%$
	Max Input Power: 50 W
	Input Impedance: $50\ \Omega$
	Polarization Type: Vertical
	Cable Insertion Loss: $< 1\text{ dB}$ ( $< 1\text{ GHz}$ )
	Cable Insertion Loss: $< 1.5\text{ dB}$ ( $1\sim 2.3\text{ GHz}$ )
	Cable Insertion Loss: $< 2\text{ dB}$ ( $2.3\text{ GHz}$ )

### 5.4. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by Hirose.

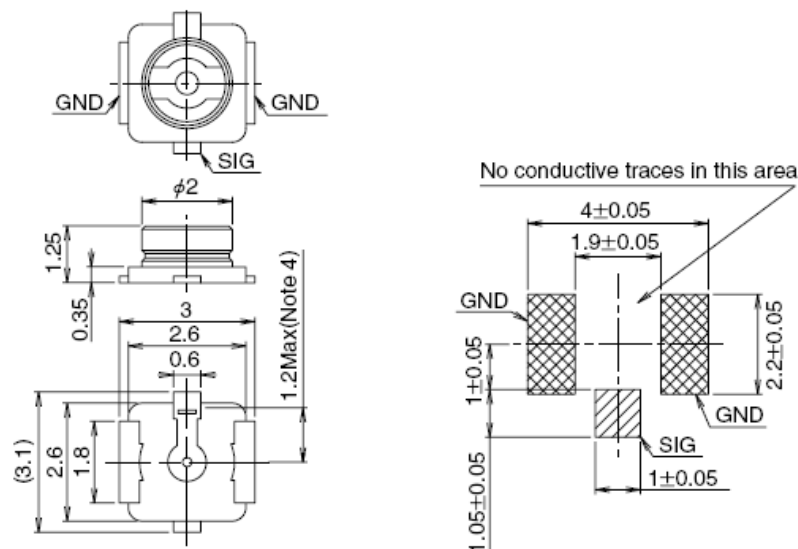
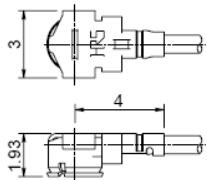
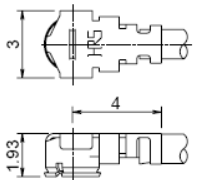
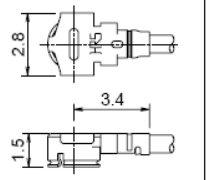
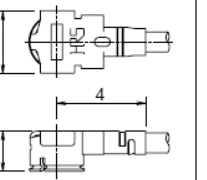
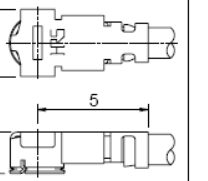


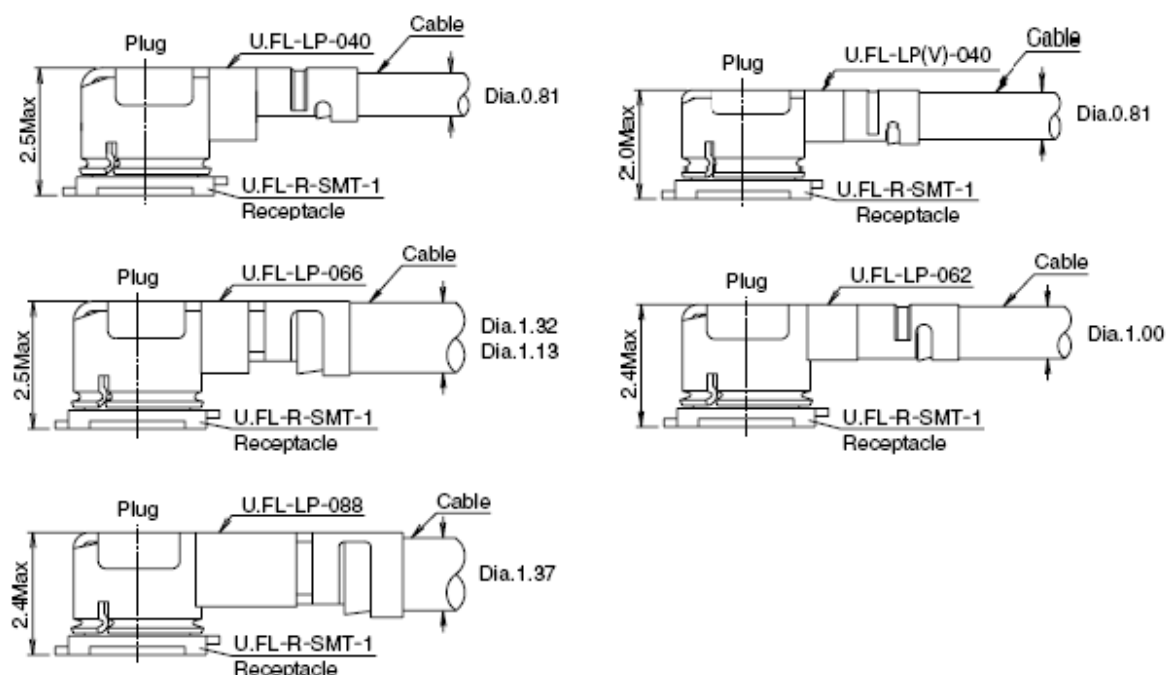
Figure 32: Dimensions of U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

**Figure 33: Mechanicals of U.FL-LP Connectors**

The following figure describes the space factor of mated connector.



**Figure 34: Space Factor of Mated Connector (Unit: mm)**

For more details, please visit <http://hirose.com>.

# 6 Electrical Characteristics & Reliability

## 6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

**Table 29: Absolute Maximum Ratings**

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	1	A
Peak Current of VBAT_RF	0	2.5	A
Voltage on Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT	V
Voltage at ADC1	0	VBAT	V

## 6.2. Power Supply Ratings

Table 30: The Module's Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must stay between the minimum and maximum values.	3.3	3.8	4.3	V
	Voltage drop during transmitting burst	Maximum power control level at EGSM 900	-	-	400	mV
I <sub>VBAT_RF</sub>	Peak supply current (during transmission slot)	Maximum power control level at EGSM 900	-	1.7	2.5	A
USB_VBUS	USB connection detect		3.5	5.0	5.25	V

## 6.3. Power Consumption

Table 31: The Module Power Consumption

EG915U-EU			
Description	Conditions	Typ.	Unit
OFF state	Power down	43	uA
	AT+CFUN=0 (USB OFF)	1.01	mA
	AT+CFUN=0 (USB ON)	2.2	mA
	AT+CFUN=4 (USB OFF)	1.02	mA
Sleep state	AT+CFUN=4 (USB ON)	2.21	mA
	EGSM @ DRX = 2 (USB OFF)	2.09	mA
	EGSM @ DRX = 5 (USB OFF)	1.55	mA
	EGSM @ DRX = 5 (USB ON)	2.67	mA

	EGSM @ DRX = 9 (USB OFF)	1.39	mA
	DCS @ DRX = 2 (USB OFF)	2.1	mA
	DCS @ DRX = 5 (USB OFF)	1.5	mA
	DCS @ DRX = 5 (USB ON)	2.78	mA
	DCS @ DRX = 9 (USB OFF)	1.36	mA
	LTE-FDD @ PF = 32 (USB OFF)	3.49	mA
	LTE-FDD @ PF = 64 (USB OFF)	2.22	mA
	LTE-FDD @ PF = 64 (USB ON)	3.48	mA
	LTE-FDD @ PF = 128 (USB OFF)	1.63	mA
	LTE-FDD @ PF = 256 (USB OFF)	1.34	mA
Idle state	EGSM @ DRX = 5 (USB OFF)	12.05	mA
	EGSM @ DRX = 5 (USB ON)	27.3	mA
	LTE-FDD @ PF = 64 (USB OFF)	12.38	mA
	LTE-FDD @ PF = 64 (USB ON)	27.58	mA
LTE data transfer	LTE-FDD B1 @ 22.29 dBm	638	mA
	LTE-FDD B3 @ 22.88 dBm	617	mA
	LTE-FDD B5 @ 23.01 dBm	637	mA
	LTE-FDD B7 @ 22.95 dBm	793	mA
	LTE-FDD B8 @ 23.17 dBm	696	mA
	LTE-FDD B20 @ 23.05 dBm	516	mA
	LTE-FDD B28 @ 23.06 dBm	559	mA
GPRS data transfer	GSM850 4DL/1UL @ 32.96 dBm	266	mA
	GSM850 3DL/2UL @ 30.7 dBm	394	mA
	GSM850 2DL/3UL @ 28.66 dBm	457	mA
	GSM850 1DL/4UL @ 26.41 dBm	464	mA

	GSM900 4DL/1UL @ 32.31 dBm	245	mA
	GSM900 3DL/2UL @ 30.7 dBm	371	mA
	GSM900 2DL/3UL @ 28.66 dBm	445	mA
	GSM900 1DL/4UL @ 26.63 dBm	452	mA
	DCS1800 4DL/1UL @ 29.84 dBm	171	mA
	DCS1800 3DL/2UL @ 27.89 dBm	242	mA
	DCS1800 2DL/3UL @ 25.85 dBm	269	mA
	DCS1800 1DL/4UL @ 23.78 dBm	279	mA
	PCS1900 4DL/1UL @ 29.68 dBm	171	mA
	PCS1900 3DL/2UL @ 27.74 dBm	247	mA
	PCS1900 2DL/3UL @ 25.66 dBm	279	mA
	PCS1900 1DL/4UL @ 23.59 dBm	295	mA
GSM voice call	GSM850 PCL=5 @ 32.82 dBm	289	mA
	GSM850 PCL=12 @ 19.08 dBm	111	mA
	GSM850 PCL=19 @ 6.12 dBm	80	mA
	GSM900 PCL=5 @ 32.34 dBm	261	mA
	GSM900 PCL=12 @ 19.06 dBm	109	mA
	GSM900 PCL=19 @ 5.39 dBm	79	mA
	DCS1800PCL=0 @ 29.89 dBm	196	mA
	DCS1800PCL=7 @ 15.96 dBm	91	mA
	DCS1800PCL=15 @ 0.95 dBm	75	mA
	PCS1900PCL=0 @ 29.66 dBm	193	mA
	PCS1900PCL=7 @ 15.59 dBm	93	mA
	PCS1900PCL=15 @ 0.58 dBm	75	mA

## 6.4. ESD

The module is not protected against electrostatics discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module, for example, ESD protection should be added at the interface of circuit design and the points that are vulnerable to electrostatic discharge damage or influence; anti-static gloves should be worn during production, etc.

ESD characteristics of the module's pins are as follows:

**Table 32: Electrostatics Discharge Characteristics (25 °C, 45 % Relative Humidity)**

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Antenna Interface	±4	±8	kV
Other Interfaces	±0.5	±1	kV

## 6.5. Operating and Storage Temperatures

**Table 33: Operating and Storage Temperatures**

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range <sup>4</sup>	-35	+25	+75	°C
Extended Operating Temperature Range <sup>5</sup>	-40	+25	+85	°C
Storage temperature range	-40	+25	+95	°C

<sup>4</sup> Within operating temperature range, the module is 3GPP compliant.

<sup>5</sup> Within extended operating temperature range, proper mounting, heating sinks and active cooling may be required to make certain functions of the module such as voice, SMS, data transmission to be realized. Only one or more parameters like Pout might reduce in their value and exceed the specified tolerances. When the temperature returns to normal operating temperature levels, the module will meet 3GPP specifications again.

# 7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are  $\pm 0.2$  mm unless otherwise specified.

## 7.1. Mechanical Dimensions

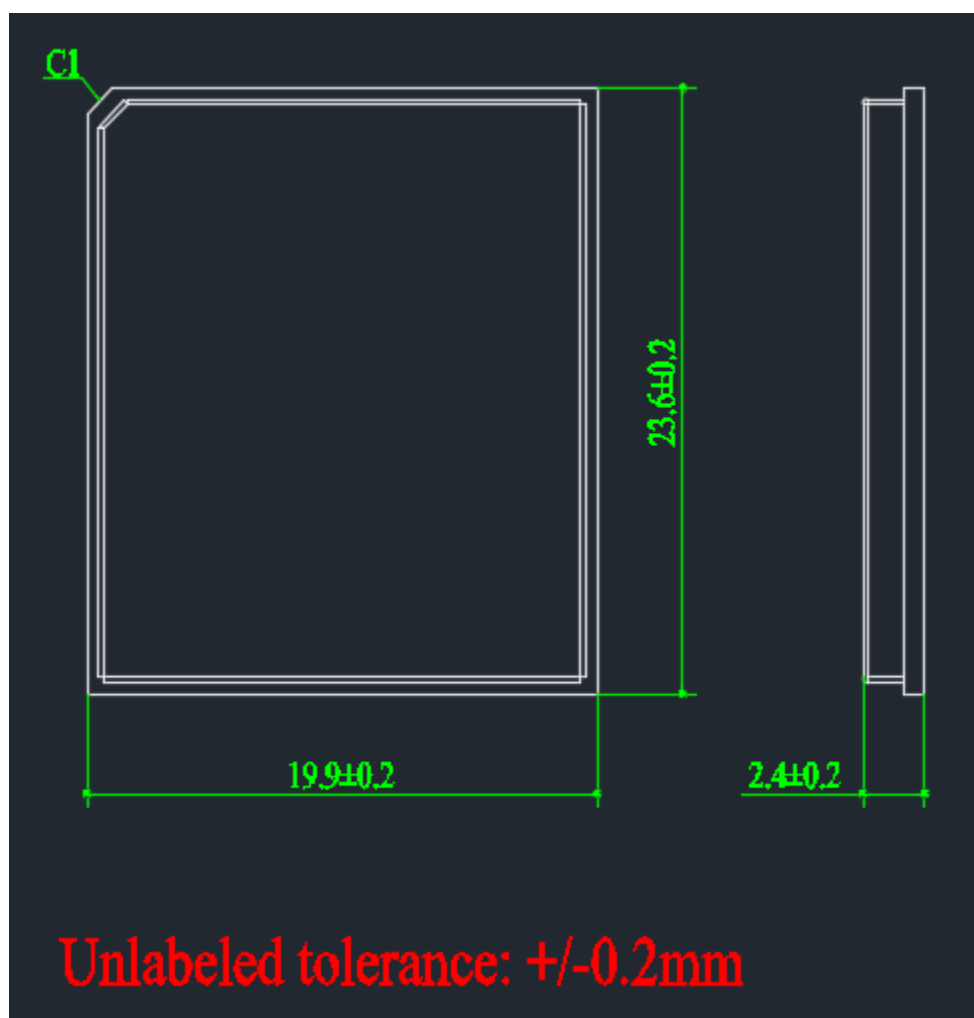
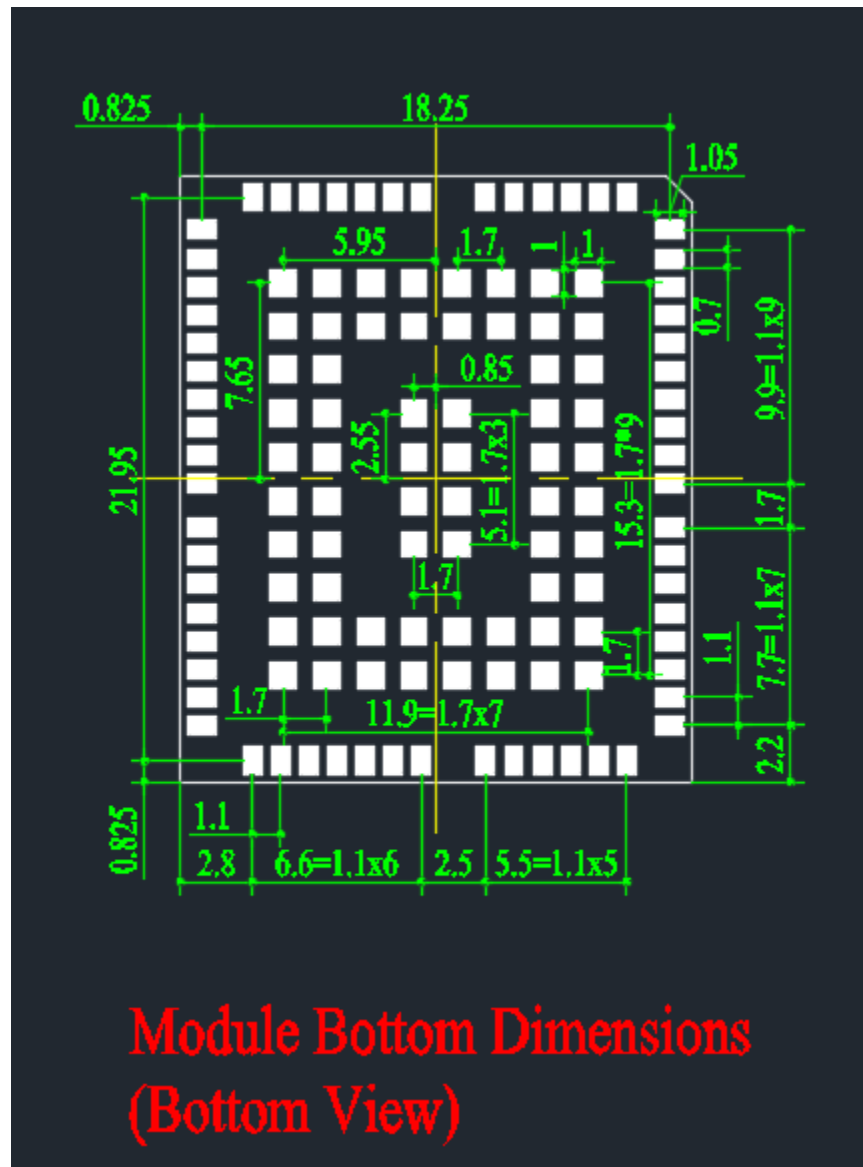


Figure 35: Module Top and Side Dimensions (Unit: mm)





### Figure 36: Module Bottom Dimensions

## NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

## 7.2. Recommended Footprint

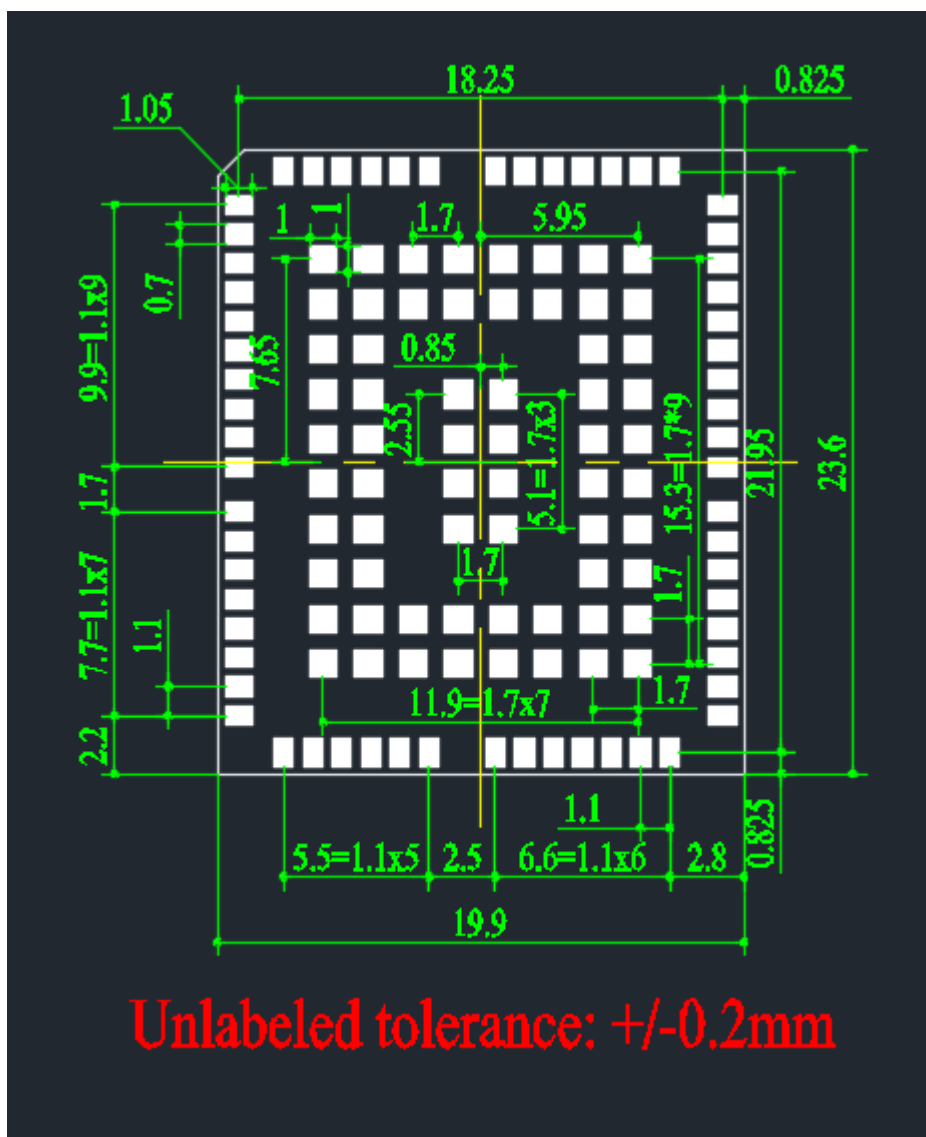


Figure 37: Recommended Footprint (TOP View)

### NOTE

1. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.
2. To keep the reliability of the mounting and soldering, keep the motherboard thickness as at least 1.2 mm.

### 7.3. Top and Bottom Views

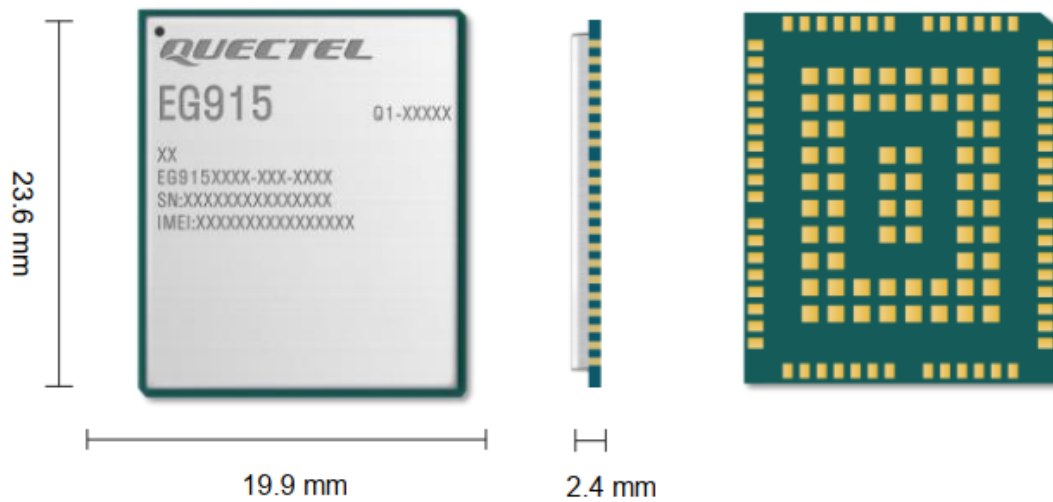


Figure 38: Top View of the Module

#### NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

# 8 Storage, Manufacturing & Packaging

## 8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be  $23 \pm 5$  °C and the relative humidity should be 35–60 %.
2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.
3. The floor life of the module is 24 hours in a plant where the temperature is  $23 \pm 5$  °C and relative humidity is below 60 %<sup>6</sup>. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 24 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).
4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:
  - The module is not stored in Recommended Storage Condition;
  - Violation of the third requirement above occurs;
  - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
  - Before module repairing.
5. If needed, the pre-baking should follow the requirements below:
  - The module should be baked for 8 hours at  $120 \pm 5$  °C;
  - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

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<sup>6</sup> This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

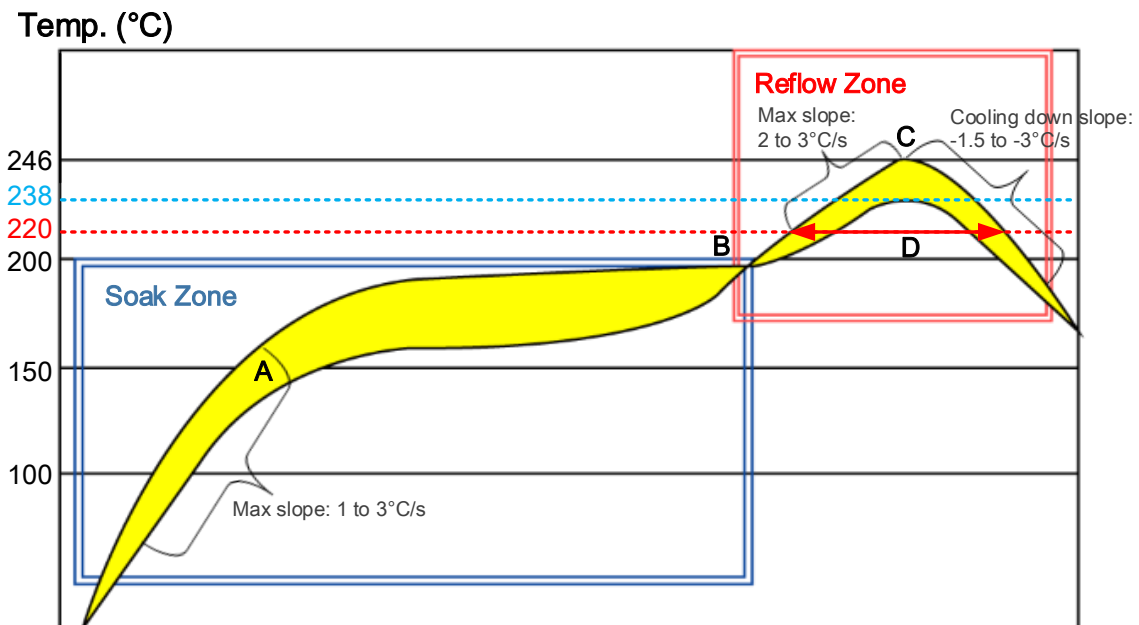
**NOTE**

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. All modules must be soldered to PCB within 24 hours after the baking, otherwise put them in the drying oven. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

## 8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.18 mm–0.20 mm. For more details, please refer to **document [4]**.

The peak reflow temperature should be 238–246 °C, with 246 °C as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.



**Figure 39: Recommended Reflow Soldering Thermal Profile**

Table 34: Recommended Thermal Profile Parameters

Factor	Recommendation
<b>Soak Zone</b>	
Max slope	1 to 3 °C/s
Soak time (between A and B: 150 °C ~ 200 °C)	70 to 120 s
<b>Reflow Zone</b>	
Max slope	2 to 3 °C/s
Reflow time (D: over 220 °C)	45 to 70 s
Max temperature	238 to 246 °C
Cooling down slope	-1 to 4 °C/s
<b>Reflow Cycle</b>	
Max reflow cycle	1

#### NOTE

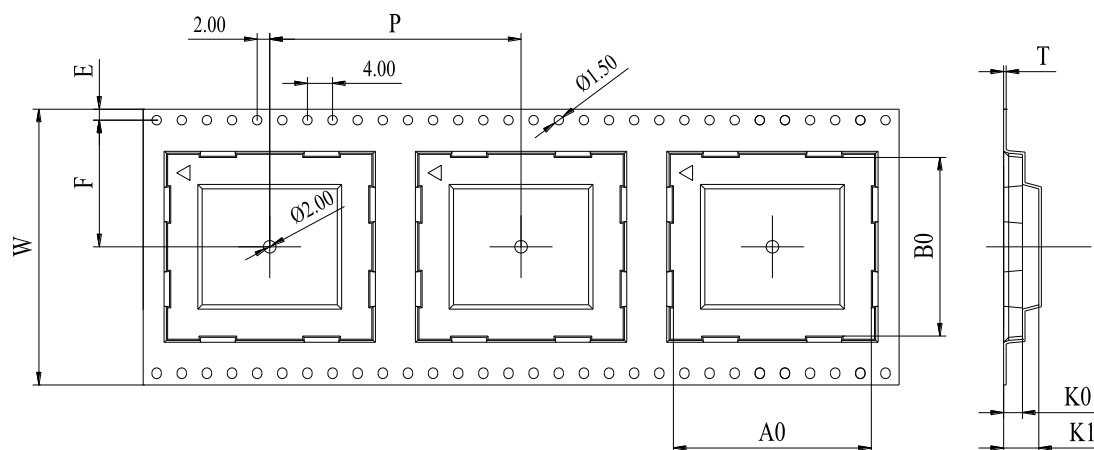
1. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
2. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
4. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
5. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in **document [4]**.

## 8.3. Packaging Specification

The module adopts carrier tape packaging and details are as follow:

### 8.3.1. Carrier Tape

Dimension details are as follow:

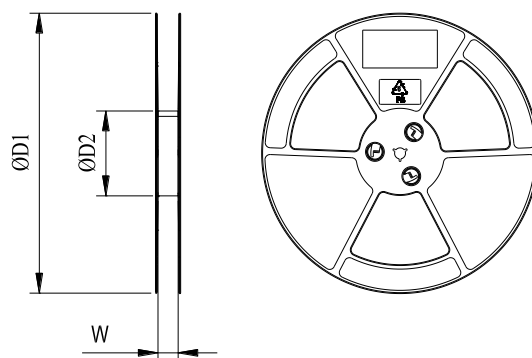


**Figure 40: Carrier Tape Dimension Drawing**

**Table 35: Carrier Tape Dimension Table (Unit: mm)**

W	P	T	A0	B0	K0	K1	F	E
44	32	0.35	20.2	24	3.15	6.65	20.2	1.75

### 8.3.2. Plastic Reel

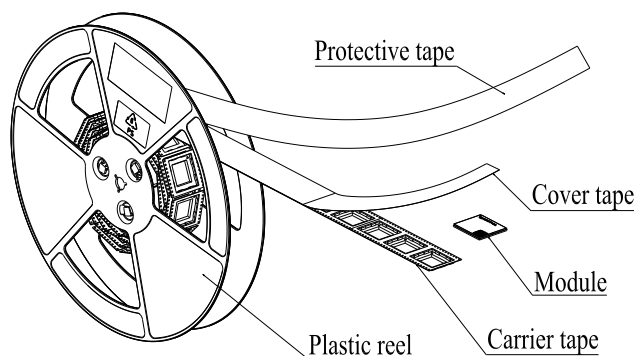


**Figure 41: Plastic Reel Dimension Drawing**

Table 36: Plastic Reel Dimension Table (Unit: mm)

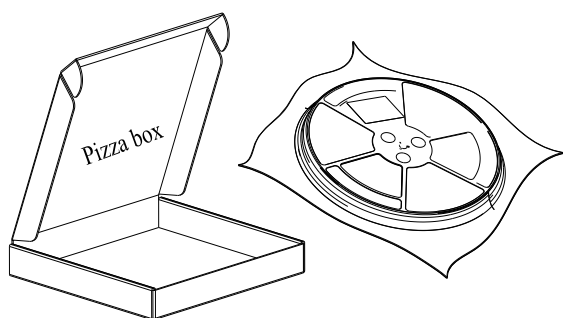
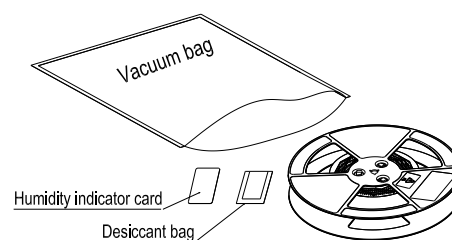
øD1	øD2	W
330	100	44.5

### 8.3.3. Packaging Process



Place the module into the carrier tape and use the cover tape to cover it; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. 1 plastic reel can load 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, vacuumize it.



Place the vacuum-packed plastic reel into the pizza box.

Put 4 packaged pizza boxes into 1 cartoon box and seal it. 1 cartoon box can pack 1000 modules.

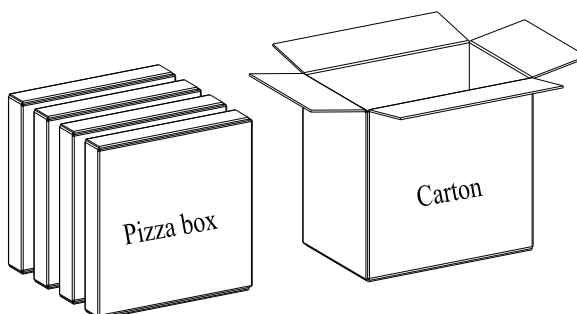


Figure 42: Packaging Process



# 9 Appendix References

**Table 37: Related Documents**

Document Name
[1] Quectel_UMTS&LTE_EVB_User_Guide
[2] Quectel_EG915U-EU_Series_AT_Commands_Manual
[3] Quectel_RF_Layout_Application_Note
[4] Quectel_Module_SMT_User_Guide

**Table 38: Terms and Abbreviations**

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR-WB	Adaptive Multi-Rate Wideband
AP	Application Processor
bps	Bits Per Second
CA	Carrier Aggregation
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CTS	Clear To Send
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DRX	Discontinuous Reception

DRX	Diversity Receive
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FR	Full Rate
GLONASS	Global Navigation Satellite System (Russia)
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GRFC	General RF Controller
HR	Half Rate
IC	Integrated Circuit
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
I/O	Input/Output
Inorm	Normal Current
LED	Light Emitting Diode
LGA	Land Grid Array
LTE	Long Term Evolution
MCU	Microcontroller Unit
MO	Mobile Originated
MS	Mobile Station
PAP	Password Authentication Protocol
PCB	Printed Circuit Board

PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PHY	Physical Layer
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RI	Ring Indicator
RF	Radio Frequency
SA	Stand Alone
SD	Secure Digital
SIMO	Single Input Multiple Output
SMS	Short Message Service
SPI	Serial Peripheral Interface
TDD	Time Division Duplexing
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	Universal Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
V <sub>max</sub>	Maximum Voltage
V <sub>nom</sub>	Nominal Voltage
V <sub>min</sub>	Minimum Voltage
V <sub>IHmax</sub>	Maximum High-level Input Voltage

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$V_{IHmin}$	Minimum High-level Input Voltage
$V_{ILmax}$	Maximum Low-level Input Voltage
$V_{ILmin}$	Minimum Low-level Input Voltage
$V_{Imax}$	Absolute Maximum Input Voltage
$V_{Imin}$	Absolute Minimum Input Voltage
$V_{OHmax}$	Maximum High-level Output Voltage
$V_{OHmin}$	Minimum High-level Output Voltage
$V_{OLmax}$	Maximum Low-level Output Voltage
$V_{OLmin}$	Minimum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio

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